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=> D HIS

     (FILE 'HOME' ENTERED AT 14:49:40 ON 07 JAN 2002)

     FILE 'REGISTRY' ENTERED AT 14:50:03 ON 07 JAN 2002
L1           476 S (SI AND O)/ELS AND 2/ELC.SUB
L2           425 S (SI AND N)/ELS AND 2/ELC.SUB
L3           318 S (SI AND O AND N)/ELS AND 3/ELC.SUB
                 E ALUMINUM/CN
                 E TUNGSTEN/CN
L4             1 S E3
                 E COPPER/CN
L5             1 S E3
                 E CHROMIUM/CN
L6             1 S E3
                 E GOLD/CN
L7             1 S E3
                 E PLATINUM/CN
L8             1 S E3
                 E PALLADIUM/CN
L9             1 S E3
                 E GERMANIUM/CN
L10            1 S E3
                 E SELENIUM/CN
L11            1 S E3

     FILE 'HCAPLUS' ENTERED AT 14:59:17 ON 07 JAN 2002
                 E POLYIMIDE/CT
                 E E3+ALL/CT
L23      1470020 S (ALUMINUM OR AL OR TUNGSTEN OR W)
L24      1274581 S (COPPER OR CU OR CHROMIUM OR CR ORGOLD OR AU)
L25       399796 S (PLATINUM OR PT OR PALLADIUM OR PD)
L26       258610 S (SELENIUM OR SE OR GERMANIUM OR GE)
L27        36496 S SILICON(W)OXIDE OR SI(W)OXIDE OR SIO OR (OXOSILYLENE(W)28SI )
L28        67146 S SILICON(W)NITRIDE OR SI(W)NITRIDE OR SIN OR (SILICON(2N) MONO
L29         7537 S ((SILICON (N)NITRIDE(N) OXIDE) OR (SILICON (N)NITRIDE(N) OXID
L30        55621 S DIAMOND OR (DIAMOND(3N)CARBON)
L31         1376 S ((FLUORIN?)(W) (DOP?)(W) (OXIDE?) OR (F)(W)(DOP?) OR (FLUORIN
L32          594 S ANTI(W)FUSE# OR ANTIFUSE# OR OTP OR ((ONE)(N)(TIME)(N)(PROGRA
L33       304000 S (DIELECTRIC? OR OXIDE OR INSULAT?)(3N)(FILM# OR LAYER? OR COA
L34      2663193 S (ANTI(N)REFLECT? OR (COAT#### OR FILM# OR LAYER?)) OR ((DICHR

     FILE 'REGISTRY' ENTERED AT 15:08:11 ON 07 JAN 2002
                 E DIAMOND/CN
L35            1 S E3

     FILE 'HCAPLUS' ENTERED AT 15:08:30 ON 07 JAN 2002
L36        31653 S L35
                 E COMPOUND SEMICONDUCTOR/CT
                 E E4
                 E E3+ALL/CT
L37         1119 S E2

     FILE 'REGISTRY' ENTERED AT 15:15:35 ON 07 JAN 2002

     FILE 'REGISTRY' ENTERED AT 15:17:27 ON 07 JAN 2002
L38       256169 S PACR/PCT
L39       251968 S L38 AND POLY?
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L40        30979 S L39 AND METHACRYLATE?
L41        31175 S L38 AND METHACRYLATE?
L42        31175 S L40 OR L41

     FILE 'HCAPLUS' ENTERED AT 15:19:41 ON 07 JAN 2002
L43       139520 S L42
L44         2368 S POLYMETHYLMETHACRYLATE

     FILE 'REGISTRY' ENTERED AT 15:28:46 ON 07 JAN 2002
L45        45348 S PI/PCT
L46        73701 S PA/PCT
                 E PARALYENE
                 E PARALYENE/CN

     FILE 'HCAPLUS' ENTERED AT 15:29:52 ON 07 JAN 2002
L47        28418 S L45
L48          158 S L32 AND L33

     FILE 'REGISTRY' ENTERED AT 15:53:22 ON 07 JAN 2002
                 E DIAMOND/CN
L49            1 S E3

     FILE 'HCAPLUS' ENTERED AT 15:53:42 ON 07 JAN 2002
L50           38 S L48 AND (VIA OR VIAS)
L51           14 S L50 AND (L49 OR L1 OR L2 OR L27 OR L28 OR L30 OR L31)
L52           64 S L48 AND (L49 OR L1 OR L2 OR L27 OR L28 OR L30 OR L31)
L53           54 S L48 AND (TRENCH? OR HOLE? OR GROOVE# OR CHANNEL OR EDGE? OR F
L54           23 S L53 AND (L49 OR L1 OR L2 OR L27 OR L28 OR L30 OR L31)
L55            1 S L48 AND (L45 OR POLYIMIDE? OR L46 OR POLYAMIDE? OR PARALYENE)
L56            0 S L48 AND L44
L57           73 S L50 OR L53
L58           45 S L57 AND (L1-L8 OR L23 OR L24 OR L25 OR GOLD OR AU)
L59           73 S L57 AND (L1 OR L2 OR L27 OR L28 OR (AMORPHOUS(N)(SI OR SILICO
L60           22 S (L52 AND L59 AND L54 AND L58)
L61           30 S L51 OR L54
L62           30 DUP REMOVE L61 (0 DUPLICATES REMOVED)
L63            0 S L60 NOT L61
L64           30 S L61 OR L60
L65           30 S L51 OR L64
                 S L48 AND (PARALYENE/CN)

     FILE 'REGISTRY' ENTERED AT 17:11:14 ON 07 JAN 2002
L66            0 S PARALYENE/CN

     FILE 'HCAPLUS' ENTERED AT 17:11:16 ON 07 JAN 2002
L67            0 S L66
L68            0 S L48 AND ( L67 )

     FILE 'REGISTRY' ENTERED AT 17:11:43 ON 07 JAN 2002
L69            0 S PARALYENE

     FILE 'HCAPLUS' ENTERED AT 17:12:50 ON 07 JAN 2002
L70            1 S PARALYENE
L71          808 S PARYLENE

     FILE 'REGISTRY' ENTERED AT 17:17:15 ON 07 JAN 2002
L72            1 S PARYLENE/CN

     FILE 'HCAPLUS' ENTERED AT 17:17:34 ON 07 JAN 2002
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=> S L48 AND(L72 OR L71)
          1051 L72
L73          0 L48 AND(L72 OR L71)
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L64 ANSWER 1 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:868915 HCAPLUS
DN 136:14099
TI **One time programmable** read only memory
IN Chang, Kuang-yeh
PA Taiwan
SO U.S. Pat. Appl. Publ., 9 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001045594	A1	20011129	US 1999-239033	19990127

AB Provided is a 1 time programmable read only memory, which includes a floating gate, an inter-metal **dielec. layer** and a control gate stacked on each other on a substrate. Also, ion-implanted regions are formed in the substrate on both sides of the stacked gate structure, and are covered by metal silicide **layers**. The inter-metal **dielec. layer** comprises an **oxide layer** and a **Si nitride layer**, in which the **oxide layer** covers the floating gate, and the **Si nitride layer** further covers the floating gate and the metal silicide **layer**. The control gate covers the **Si nitride layer**. Also, the 1 time programmable read only memory of the invention not only can reduce the elec. resistance of bit lines and enhance its own performance, but also has a small size and a greater planarity due to an absence of field **oxide layers** and contact windows formed thereon and therein.

L64 ANSWER 2 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:691691 HCAPLUS
DN 135:234905
TI Procedure for manufacturing a wiring plane on a semiconductor chip with an **antifuse**.
IN Lehr, Matthias; Leiberg, Wolfgang
PA Infineon Technologies A.-G., Germany
SO Ger., 8 pp.
CODEN: GWXXAW
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 10021098	C1	20010920	DE 2000-10021098	20000420
EP 1148542	A2	20011024	EP 2001-107218	20010323
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				

PRAI DE 2000-10021098 A 20000420
AB According to the invention a buried **anti-reflection layer** is used in a **dielec. layer** with the prodn. of a wiring plane on a semiconductor chip with **antifuses**, in which **via holes** are formed which are used for optical lithog. to form line drains over the **via holes** by using one-step etching only.
RE.CNT 5

L64 ANSWER 3 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:537446 HCAPLUS
DN 135:101076
TI Method of making a barrier **layer** to protect programmable **antifuse** structure from damage during fabrication sequence
IN Hsu, Woan Jen; Liu, Chi Kang
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6265257	B1	20010724	US 1999-409877	19991001

AB A method for forming an **antifuse** interconnect structure, for a 1-time fusible link, to be used with field-programmable gate arrays, has been developed. The process features the use of an **amorphous Si layer**, used as the **antifuse layer**, with the **amorphous Si layer** protected by a thin barrier **layer**, during the patterning procedure. The protected **antifuse layer** results in a reproducible thickness, and thus reproducible pulsing voltages, needed for rupturing of the **antifuse layer**. Planarization of an underlying metal plug, **via** a conductor **layer** refill procedure, offers a smooth top surface, **flush** with the top surface of the adjacent interlevel **dielec**. **layer**, for the overlying **antifuse layer**.

L64 ANSWER 4 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:464313 HCAPLUS
DN 135:39751
TI Method of making a dual damascene **anti-fuse** prior to **via** fabrication without using dedicated lithographic masking levels
IN Radens, Carl J.; Brintzinger, Axel C.
PA International Business Machines Corporation, USA; Infineon Technologies North America Corp.
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6251710	B1	20010626	US 2000-560072	20000427
JP 2001358224	A2	20011226	JP 2001-133328	20010427
US 2001036750	A1	20011101	US 2001-873537	20010604
PRAI US 2000-560072	A	20000427		

AB An interconnect structure in which a patterned **antifuse** material is formed therein comprising: a substrate having a 1st level of elec. conductive features; a patterned **anti-fuse** material, formed on said substrate, wherein said patterned **anti-fuse** material includes an opening to at least one of said 1st level of elec. conductive features; a patterned interlevel **dielec**. **material** formed on said patterned **anti-fuse** material, wherein said patterned interlevel dielec. includes **vias**, as least one of said **vias** includes a **via** space; and a 2nd level of elec. conductive features formed in said **vias** and

via spaces.

L64 ANSWER 5 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:449934 HCAPLUS
DN 135:39676
TI Design and fabrication of a dielectric-based **anti-fuse** cell with a polysilicon contact plug
IN Bergemont, Albert; Kalnitsky, Alexander
PA National Semiconductor Corporation, USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6249010	B1	20010619	US 1998-135536	19980817

AB A dielec.-based **anti-fuse** cell and cell array, that include a doped polysilicon contact plug, with a low resistance in the programmed state, a low capacitance, and a small cell area. The dielec.-based **anti-fuse** cell includes a 1st **insulating layer**, typically SiO2, on the surface of a semiconductor substrate. A 1st doped polysilicon (poly 1) **layer** is on the upper surface of the 1st **insulating layer** and a 2nd **insulating layer** is over the poly 1 **layer**. A doped polysilicon contact plug extends through the 2nd **insulating layer** and into the poly 1 **layer**. A **dielec. layer**, typically either an ONO or NO **dielec.** composite **layer**, covers the upper surface of the doped polysilicon contact plug. A 2nd doped polysilicon (poly 2) **layer** is disposed on the **dielec. layer**. A process for manufg. the **anti-fuse** cell and array includes 1st providing a semiconductor substrate and forming a 1st **insulating layer** on its surface. Next a poly 1 **layer** (e.g. bit lines) is formed on the surface of the 1st **insulating layer** followed by the formation of a 2nd **insulating layer** over the poly 1 **layer**. A contact opening that extends into the poly 1 **layer** is then created in the 2nd **insulating layer** and filled with a doped polysilicon contact plug. Next, a **dielec. layer** is formed on the upper surface of the doped polysilicon contact plug, followed by the formation of a poly 2 **layer** (e.g. word lines) on the upper surface of the **dielec. layer**

L64 ANSWER 6 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:90366 HCAPLUS
DN 130:132793
TI Double half **via antifuse** fabricated with low sensitivity to selective etching during **via** formation
IN McCollum, John L.
PA Actel Corporation, USA
SO U.S., 7 pp., Cont.-in-part of U.S. 5,552,627.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 6

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5866937	A	19990202	US 1995-482270	19950607
	US 5070384	A	19911203	US 1990-508306	19900412
	US 5181096	A	19930119	US 1990-604779	19901026
	JP 04226068	A2	19920814	JP 1991-171589	19910412
	JP 3095811	B2	20001010		
	JP 04282864	A2	19921007	JP 1991-305470	19911024
	US 5411917	A	19950502	US 1993-4912	19930119

B An **antifuse** comprises a substantially planar conductive lower electrode covered by a 1st **layer** of **Si nitride** . A **layer** of **amorphous Si** is disposed over the **Si nitride layer**. A 1st **dielec** . **layer** is disposed over the surface of the **amorphous Si layer** and has a 1st aperture there through communicating with the **amorphous Si layer**. A 2nd **layer** of **Si nitride** is disposed over the 1st **dielec**. **layer** and in the 1st aperture. A conductive upper electrode, such as a **layer** of Ti nitride, is disposed over the 2nd **layer** of **Si nitride**. A 2nd **dielec**. **layer** is disposed over the surface of the conductive upper electrode and has a 2nd aperture there through in alignment with the 1st aperture communicating with the conductive upper electrode. An overlying metal **layer** is disposed over the surface of the 2nd **dielec**. **layer** and in the 2nd aperture making elec. contact with the conductive upper electrode.
RE.CNT 5

L64 ANSWER 7 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:77382 HCAPLUS
DN 130:132765
TI Semiconductor nonvolatile memory device and manufacture thereof
IN Araki, Hitoshi; Hatakeyama, Masao
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 15 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11026620	A2	19990129	JP 1998-75343	19980324
PRAI	JP 1997-116753		19970507		

AB The invention relates to a semiconductor nonvolatile memory cell, e.g., a PROM, an **OTP** (one time PROM), an EEPROM, a flash EEPROM, wherein the degrdn. of tunnel **oxide film** at the **trench**

corner or the LOCOS **edge** is minimized.

L64 ANSWER 8 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:34438 HCAPLUS
DN 130:89329
TI Fabricating an amorphous silicon **antifuse** structure
IN Love, Michela S.; Parks, Delbert H.
PA VLSI Technology, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5856213	A	19990105	US 1996-687234	19960725

AB An **antifuse** structure is formed between 2 metal contacts in which a thin **oxide layer** is formed on the 1st or bottom metal, a shallow **via** is provided in the **oxide layer**, and a **layer** of amorphous Si is deposited over the thin oxide and into the shallow **via** without leaving the usual furrows in the amorphous Si, thereby eliminating the step coverage problems of cusps forming in the subsequently applied 2nd or top metal.

L64 ANSWER 9 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:550586 HCAPLUS
DN 129:169222
TI **Antifuse**-programmed PROM cell
IN McCollum, John
PA Actel Corporation, USA
SO PCT Int. Appl., 17 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 9835387	A1	19980813	WO 1998-US2924	19980210
W: JP, KR				
RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
US 5909049	A	19990601	US 1997-797202	19970211
EP 976158	A1	20000202	EP 1998-905091	19980210
R: DE, FR, GB, IT				
PRAI US 1997-797202		19970211		
WO 1998-US2924		19980210		

AB An **antifuse**-based PROM cell design allows large currents to be sinked during cell programming to ensure low programmed resistance of the cell while using min.-geometry select devices. This is achieved by using a pseudo-SCR latchup effect during programming. The regions in the semiconductor substrate forming lower **antifuse** electrodes for the **antifuses** in the PROM cells are doped at low levels with P. An **antifuse layer** formed from an **oxide**, oxide-nitride, or **oxide**-nitride-**oxide antifuse layer** is formed over the lower **antifuse** electrode, and an upper **antifuse** electrode is formed from polysilicon. A min.-geometry N-**channel** select transistor is formed in series with the **antifuse** to complete the PROM cell. The drain and source diffusions of the select transistor are As-doped and the drain diffusion is contiguous with the lower **antifuse** electrode. A

bit line is contacted to the upper **antifuse** electrode and the select transistor gate is part of a polysilicon word line. The source diffusion of the select transistor is grounded.

L64 ANSWER 10 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:199628 HCAPLUS
DN 128:264874
TI Semiconductor devices having an **antifuse** built in an integrated circuit for field programmable gate arrays
IN Sakurai, Koji; Yuasa, Hiroshi; Yamaoka, Toru; Honta, Koji
PA Matsushita Electronics Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10084043	A2	19980331	JP 1996-237474	19960909

AB The title devices comprise a 1st interlayer **insulator film** formed on a semiconductor substrate, a contact **hole** provided through the 1st interlayer **insulator film** and reached to the substrate, a 1st metallic circuit **layer** connected to the substrate through the contact **hole**, a 2nd interlayer **insulator film** covering over the 1st circuit **layer** and on the 1st interlayer **insulator film** , a 2nd metallic circuit formed on the 2nd interlayer **insulator film**, an **antifuse film** formed on the 2nd metallic circuit **layer**, and a 3rd metallic circuit **layer** formed on the **antifuse**. The **antifuse film** bound between the 2nd and 3rd metallic circuit **layers** are leveled so as to give precision controlled **antifuse** characteristics such as insulative breakdown voltage.

L64 ANSWER 11 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:180602 HCAPLUS
DN 128:224871
TI **Antifuses** and stacked capacitors in integrated circuits and blowing of the **antifuses**
IN Dennison, Charles H.
PA Micron Technology, Inc., USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5726483	A	19980310	US 1995-503022	19950717
	US 5756393	A	19980526	US 1997-822991	19970321
	US 6146925	A	20001114	US 1998-14766	19980128
	US 6221729	B1	20010424	US 1998-83624	19980522
	US 6291871	B1	20010918	US 1999-244557	19990203
PRAI	US 1995-503022	A3	19950717		
	US 1997-822991	A1	19970321		
	US 1998-14766	A3	19980128		

AB A method of jointly forming stacked capacitors and **antifuses** includes (a) providing a common **layer** of elec. conductive material to form both a capacitor storage node and an inner

antifuse plate; (b) providing a common **layer** of **dielec. material** over the capacitor storage node and the inner **antifuse** plate, the common **layer** of **dielec. material** comprising both an intervening capacitor dielec. element and an intervening **antifuse dielec.** element, the common **layer** of **dielec. material** having a 1st breakdown voltage per unit length for a given current per unit area; (c) providing a common **layer** of elec. conductive material over the common **layer** of **dielec. material** to form both a capacitor cell **layer** and an outer **antifuse** plate; (d) providing a lateral **edge** of the outer **antifuse** plate and a lateral **edge** of the intervening **antifuse** dielec. element; and (e) depositing an **antifuse** breakdown **layer** of **dielec. material** over the lateral **edges** of the outer **antifuse** plate and the intervening **antifuse** dielec. element, the **antifuse** breakdown **layer** having a 2nd breakdown voltage per unit length for the same given current per unit area, which is lower than the 1st breakdown voltage per unit length. Novel **antifuse** constructions, integrated circuits, and blowing of **antifuses** are also disclosed.

L64 ANSWER 12 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:180640 HCAPLUS
DN 126:180005
TI Semiconductor device containing **antifuses** with good flatness and its manufacture
IN Yamazaki, Satoshi
PA Yamagata Nippon Denki Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08330530	A2	19961213	JP 1995-133672	19950531
	JP 2648134	B2	19970827		

AB The device includes an **antifuse** element contg. a contact **hole** in a laminate of: a 1st **insulating film**, an interlayer-**insulating film** contg. **SiN** and a 2nd **insulating film**, and a 1st **Al**-based wiring pattern, where a 2nd **Al**-based wiring pattern is formed on the 1st wiring pattern at the **hole** bottom **via** a 3rd **insulating film**. The 2nd **insulating film** may be polyimide. The manufg. process, including dry-etching for the contact **hole** and temp.-controlled annealing for simultaneous formation of the 2nd and the 3rd **insulating films**, is also claimed. The manuf. shows good through put.

L64 ANSWER 13 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:607555 HCAPLUS
DN 125:236087
TI **Antifuse** with a double-**via** spacer-defined contact and its manufacture
IN Iranmanesh, Ali
PA Crosspoint Solutions, Inc., USA
SO PCT Int. Appl., 25 pp.
CODEN: PIXXD2

DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9625766	A1	19960822	WO 1996-US2024	19960209
	W: JP, KR				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 5663591	A	19970902	US 1995-388673	19950214
PRAI	US 1995-388673		19950214		

AB The present invention provides for a method of forming an **antifuse** in an integrated circuit having a 1st **insulating layer** on a semiconductor substrate. The method comprises forming a 1st metal interconnection **layer** on the 1st **insulating layer**; forming a relatively thin, 2nd **insulating layer** over the 1st metal interconnection layer with a **via** where the **antifuse** is to be located to expose the 1st metal interconnection layer; forming 1st spacer regions on the sidewalls of the 2nd **insulating layer**; forming a programming **layer** on the 2nd **insulating layer** and in the **via** to contact the 1st metal interconnection line; forming 2nd spacer regions on the sidewalls of the programming layer in the **via**; forming a barrier metal layer on the programming layer; forming a relatively thick, 3rd **insulating layer** on the barrier metal layer with a 2nd aperture to expose a portion of the barrier metal layer; and forming a 2nd metal interconnection **layer** on the 3rd **insulating layer** and in the 2nd aperture to contact the portion of the barrier metal layer.

L64 ANSWER 14 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:563667 HCAPLUS
DN 125:263124
TI Electrically programmable **antifuse** incorporating dielectric and amorphous silicon interlayers
IN McCollum, John L.; Eltoukhy, Abdelshafy A.; Forouhi, Abdul R.
PA Actel Corporation, USA
SO U.S., 15 pp. Cont.-in-part of U. S. 5,411,917.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 6

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5552627	A	19960903	US 1994-231634	19940422
	US 5070384	A	19911203	US 1990-508306	19900412
	US 5181096	A	19930119	US 1990-604779	19901026

B An **antifuse** may be fabricated as a part of an integrated circuit in a **layer** located above and **insulated** from the semiconductor substrate. The **antifuse** includes a lower 1st metal electrode, a 1st **antifuse dielec. layer** (preferably **Si nitride**) on the lower 1st electrode, and an **antifuse** layer (preferably amorphous Si) on the 1st **dielec. layer**. An interlayer **dielec. layer** is disposed on the **antifuse** layer and includes an **antifuse via** formed completely through it. A 2nd **antifuse dielec. layer** (preferably **Si nitride**) is disposed over the amorphous Si layer in the **antifuse via**, and an upper 2nd metal electrode is disposed over the 2nd **dielec. layer** in the

antifuse via.

L64 ANSWER 15 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:551149 HCAPLUS
DN 125:210272
TI **Antifuse** semiconductor integrated circuits
IN Jinriki, Hiroshi; Tamura, Yoshimitsu; Kimura, Yoshitaka; Tsutsui, Che; Oota, Tomohiro; Komya, Takayuki
PA Kawasaki Steel Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 38 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08153799	A2	19960611	JP 1995-210670	19950818
	JP 3104843	B2	20001030		
	US 5565702	A	19961015	US 1994-353296	19941205
	US 5641985	A	19970624	US 1994-353294	19941205
	US 5679974	A	19971021	US 1994-353287	19941205

AB The circuit has its lower **layer** electrodes made of an amorphous conductive material. The upper **layer** electrode may be made of an amorphous conductive material. The conductive material may be (1) a compd. from .apprx.>2 of Co, Ni, **Cu**, Ti, Zr, Nb, Mo, Hf, Ta, and **W** (group 1), (2) a compd. from .apprx.>1 of Group 1 with .apprx.>1 of Si, B, N, C, **Ge**, As, P, and Sb (Group 2), or **Al**, or Y and/or La, and **Al**, (3) Y-La or a compd. from Y and/or La with **Al**, or (4) a compd. from **Au**, **Pt**, **Pd**, and/or Ag with .apprx.>1 of Group 2, .apprx.>1 of Group 1, or Y and/or La. The lower **layer** electrode may be a metal silicide with compn. ratio of the metal higher than the stoichiometric ratio. The lower and the upper **layer** electrode may be formed from a material contg. refractory metal(s) and a low m.p. metal lower in resistivity than the refractory metal(s), resp. The circuit may have (1) the lower wiring **layer** consisting of an **Al** alloy **film** and the uppermost **layer** of TiN, the lower **layer** electrode from the **Al** alloy **film** with removal of the TiN **film** in the depth direction at the bottom of the contact **hole**, **antifuse insulating films** from a SiO2, a Si3N4, or a Ta2O5 **film**, and the upper **layer** electrode with the lowermost **layer** from an **Al** alloy which forms a contact to **antifuse insulating film** of the upper wiring, or (2) the lower **layer** electrode forming a contact of the lower wiring from an **Al** or an **Al** alloy monolayer to the **antifuse insulating film**, the upper **layer** electrode from **Al** or an **Al** alloy, and the lower wiring located immediately above an **insulating film** on the substrate and elec. connected to the substrate in a contact **hole** through a barrier metal composite **film**.

L64 ANSWER 16 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:250927 HCAPLUS
DN 124:329458
TI Extremely low ON-resistance metal-to-metal **antifuses** with Al-Cu/10 nm-thick p-SiNx/Al-Cu structure for next generation very high speed FPGAs (field programmable gate arrays)
AU Tamura, Yoshimitsu; Kimura, Yoshitaka; Tsutsui, Chie; Shinriki, Hiroshi

CS Advanced Technology Research Section, Kawasaki Steel Corp., Chiba, 260, Japan
SO Jpn. J. Appl. Phys., Part 1 (1996), 35(2B), 1049-53
CODEN: JAPNDE; ISSN: 0021-4922
DT Journal
LA English
AB The authors present a novel metal-to-metal **antifuse** structure consisting of a plasma enhanced CVD **Si nitride** (p-SiNx) **dielec. film** sandwiched between two Al layers. The leakage current in the off-state is markedly reduced by using Al film as the upper electrode instead of Ti or TiN (Ti nitride) film. A Al-Cu/10 nm-thick p-SiNx/Al-Cu structure **antifuse** provides sufficient long-term off-state reliability exceeding ten years at 3.6 V while keeping low breakdown voltage (10 V). An extremely low on-resistance of .apprx.3 .OMEGA. and a narrow distribution are also realized. A new **antifuse** structure (Al-Cu/p-SiNx/Al-Cu(100 nm)/Ti/TiN/Al-Cu) highly compatible with the conventional **via** formation process in double metal interconnect wiring is proposed. This type of **antifuse** structure is very promising for next-generation very high-speed FPGAs.

L64 ANSWER 17 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:248262 HCAPLUS
DN 124:304901
TI Semiconductor integrated circuit having **antifuse** structure and its manufacture
IN Tanizaki, Yasunobu; Kobayashi, Masashi; Sawase, Terumi
PA Hitachi Ltd, Japan; Hitachi Micro System Kk
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08031944	A2	19960202	JP 1994-163504	19940715

AB In the **antifuse** structure a bottom electrode is **coated** with a **dielec. film via** a contact **hole** of an **insulator** having a controlled **film** thickness for a thickness uniformity of the **dielec. film** in the contact **hole**. The sides of the contact **hole** may be tapered. Or the bottom electrode is directly **coated** with a **dielec. film**. The top and bottom electrode may comprise silicide-forming metal (e.g., Ti, W, Mo, Ta) or its alloy and the **dielec. film** may comprise **amorphous Si**, SiO2, Si3N4, SiC or other Si compd monolayer or multilayer. The manuf. involves forming the contact **hole** by isotropic etching or directly laminating the **dielec. film** on the bottom electrode. The **antifuse** structure is useful for a FPGA (field programmable gate array).

L64 ANSWER 18 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:1002485 HCAPLUS
DN 124:72867
TI Interfacial reaction in the sputter-deposited SiO2/Ti0.1W0.9 **antifuse** system
AU Baek, Jong Tae; Park, Hyung-Ho; Cho, Kyung-Ik; Yoo, Hyung Joun; Kang, Sang Won; Ahn, Byung Tae

CS Semiconductor Technol. Div., Electr. Telecommunications Res. Inst., Taejon, 305-600, S. Korea
SO J. Appl. Phys. (1995), 78(12), 7074-9
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
AB The effects of annealing temp. on the interfacial reactions and the **antifuse** I-V characteristics of ultra thin SiO2 **layer** deposited on Ti0.1W0.9 substrate were studied. The interfacial reactions were analyzed using XPS and Auger electron spectroscopy with the sample which is in situ annealed under ultra high vacuum or ex situ annealed in a nitrogen atm. The surface of the Ti0.1W0.9 substrate was oxidized during sputter deposition of SiO2 **layer**. Ti, **W** oxides consist of Ti2O3 (Ti3O5), TiO2, WO2, and WO3. The WO3 and Ti2O3 decompd. into metallic **W** and Ti at 400 and 500.degree., resp. The breakdown voltage of the **antifuse** decreased as the annealing temp. increased, due to the thinning of **dielec. layer** resulted from the decompn. of Ti, **W** oxides and the formation of metallic **W** and Ti. Annealing at 600.degree. caused the reaction between metallic (Ti,**W**) and SiO2 **layer** and formed elemental silicon in the **dielec. layer**, where SiO2 **layer** completely lost its **dielec**. property. The breakdown of dielec. property might from a metallic **channel** in the SiO2 **film**, which mainly contains metallic **W**, Ti, and Si.

L64 ANSWER 19 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:982554 HCAPLUS
DN 124:19848
TI Method of manufacturing an **antifuse** with silicon spacers and resulting **antifuse**
IN Iranmanesh, Ali A.
PA Crosspoint Solutions, Inc., USA
SO PCT Int. Appl., 22 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9527313	A1	19951012	WO 1995-US3676	19950322
	W: JP, KR				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 5572062	A	19961105	US 1994-221344	19940331
PRAI	US 1994-221344		19940331		

AB A method and resulting **antifuse** structure in an integrated circuit include a 1st metal interconnection **layer** on a 1st **insulating layer** over the substrate of the integrated circuit and a 2nd **insulating layer** over the metal interconnection layer. The 2nd **insulating layer** has a **via** therein and a programming layer located in the **via**. Such a programming layer includes a 1st region on the 1st metal interconnection layer which is removed from sides of the 2nd **insulating layer** in the **via** and a 2nd region on the sides of the 2nd **insulating layer via** . The 1st region has substantially a 1st thickness, and the 2nd region has substantially a 2nd thickness which is greater than the 1st thickness. Upon programming the **antifuse** structure, a conducting link forms in the 1st region of the programming layer.

L64 ANSWER 20 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:503255 HCAPLUS
DN 122:304581
TI Manufacture of semiconductor devices
IN Tsuzuki, Norihisa
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07014920	A2	19950117	JP 1993-147266	19930618

AB The devices are manufd. by (1) forming **Al**(-based alloy)-contg. under **layer** wirings having diffusion prevention **layers** comprising Ti nitride, Ti tungstide, or **W** nitride on substrates, (2) **coating** the **layers** with stopper **layers** comprising high-m.p. metal silicides, (3) **coating** the wirings with SiO2-based interlayer **insulating layers**, (4) forming **via-hole** upper domains penetrating the **layers** by using resist masks with openings to bare the stopper **layers**, (5) removing of the masks, (6) removing of the bared stopper **layers** by using the interlayer **layers** as masks and the prevention **layers** as etch-stoppers by etching to bare the prevention **layers** and form **via-holes**, (7) optionally depositing amorphous thin **films** comprising **amorphous Si**, **amorphous carbon**, or Si3N4 **films** sandwiched by SiO2 **films** on the interlayer **layers** to **coat** the **via-holes**, and (8) optionally **coating** the amorphous **films** with upper **layer** wirings to form **antifuses** comprising the amorphous **films** sandwiched by the under and upper **layer** wirin

L64 ANSWER 21 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:475907 HCAPLUS
DN 123:45845
TI Semiconductor device having **antifuse** structure of field programmable gate array and its manufacture
IN Takagi, Mariko; Yoshii, Ichiro; Yasuda, Hiroo; Ikeda, Naoki; Hama, Kaoru
PA Tokyo Shibaura Electric Co, Japan; Toshiba Micro Electronics
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07022513	A2	19950124	JP 1993-190949	19930705
	CN 1107255	A	19950823	CN 1994-108287	19940705
	CN 1076123	B	20011212		
	US 5550400	A	19960827	US 1994-270458	19940705
PRAI	JP 1993-190949	A	19930705		

AB The device has (A) a semiconductor substrate **coated** with a 1st **Al** wiring elec. connected with a 1st electrode comprising a barrier metal for **Al** and a 2nd **Al** wiring elec. connected with a 2nd electrode comprising a barrier metal for **Al** and (B) a SiN0.6-1.2 **antifuse film** contacted with the both electrodes. The device has (A) a semiconductor substrate **coated** with a 1st **Al** wiring elec. connected with a barrier metal 1st electrode, (B) an elec. **insulating film** covered on the 1st wiring and the 1st electrode, (C) a SiN0.6-1.2 **antifuse film** contacted with the 1st electrode **via** a **hole** of the **insulating film**, (D) a monolayer or multilayer barrier metal 2nd electrode on the **antifuse film**, and (E) a 2nd **Al** wiring connected with the 2nd electrode on the substrate. The device is manufd. by forming a 1st **Al** wiring on a semiconductor substrate, forming a barrier metal 1st electrode elec. connected with the 1st wiring, forming an elec. **insulating film** on the 1st electrode and the 1st wiring, forming a **hole** in the **insulating film**, plasma chem. vapor depositing a SiN0.6-1.2 **antifuse film** contacted with the 1st electrode **via** the **hole**, forming a monolayer or multilayer barrier metal 2nd electrode on the **antifuse film**, and forming a 2nd **Al** wiring connected with the 2nd electrode on the substrate. The **antifuse film** showed lower **dielec**. const. than that of **amorphous Si** and high elec. resistivity. Hillock generation of the **Al** wiring was prevented.

L64 ANSWER 22 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:438087 HCAPLUS
DN 122:203166
TI **Antifuse** components and manufacturing thereof
PA Actel Corp., USA
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 6

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	JP 06224304	A2	19940812	JP 1993-247539	19930908
	US 6001693	A	19991214	US 1995-999970	19950901
PRAI	US 1992-950264	A	19920923		
	US 1994-319170	A3	19941006		

AB The components have an **antifuse layer** formed in a multilayer **channel** and are prepd. by (1) successively forming a lower electrode, a lower diffusion-barrier **layer**, a **dielec**. etching-stopper, and an isolating **dielec**. thick **layer** to give a laminated dielec. interlayer, (2) etching the dielec. interlayer to form a tapered **channel** to expose the lower electrode, (3) forming **antifuse** and upper diffusion-barrier **layers** provided in the **channel**, and (4) forming an upper electrode over the upper diffusion-barrier **layer**. The etching-stopper is Si3N4. The laminated interlayer **dielec**. **layer** may also have a SiO2 **layer**. The use of the materials for the etching-stopper and the laminated interlayer **dielec**. **layer** gives the **antifuse** components a minimized contamination on the **antifuse** material during etching.

L64 ANSWER 23 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:383068 HCAPLUS
DN 122:149475
TI Semiconductor devices and their manufacture
IN Jinriki, Hiroshi; Kaizuka, Kenji; Oota, Tomohiro
PA Kawasaki Steel Co, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 3

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06302700	A2	19941028	JP 1993-90318	19930419
US 5521423	A	19960528	US 1994-228257	19940415
PRAI JP 1993-90318		19930419		
JP 1993-90319		19930419		
JP 1993-92960		19930420		

AB The devices, contg. plural **antifuses**, consist of (A) the 2nd conductive wirings successively **coated** with (B) **insulating layers** having contact **holes** with **insulating films** consisting of **oxides** of Ti, Ta, Nb, Zr, Y, or Hf, (C) interlayer **films**, and (D) the 1st conductive wirings. Program devices, manufd. by puncturing the **insulating films** in the **holes** with resistance .ltoreq.200 .OMEGA., are also claimed. The manuf. involves (1) forming the **insulating layers** on the 1st conductive wirings comprising silicides of Ti, Ta, Nb, Zr, Hf, Co, Y, **W**, or Mo or Si, (2) forming the contact **holes** by patterning and etching, (3) forming the **insulating films**, (4) treating in acidic atm. to form the interlayer **films** with SiO2 on the interfaces of the 1st wirings and the **insulating films**, and (5) forming patterns for the 2nd wirings on the **insulating films**.

ANSWER 24 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:354704 HCAPLUS
DN 122:149444
TI Metal-to-metal **antifuse** including etch stop layer
IN Chen, Wenn Jei; Chiang, Steve S.; Hawley, Frank W.
PA USA

SO U.S., 6 pp. Cont.-in-part of U.S. Ser. No. 950,264, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 6

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5381035	A	19950110	US 1993-172132	19931221
US 5614756	A	19970325	US 1994-284054	19940801
US 5525830	A	19960611	US 1994-322871	19941012

AB Planar layers of nitride (1st nitride layer), a-Si (1st a-Si layer), nitride (2nd nitride layer) and a-Si (2nd a-Si layer) are laid down over a 1st metalization layer. A **dielec. layer** is then laid down on top of the 2nd a-Si layer. A **via** is opened in the **dielec. layer** with an etch gas which attacks a small portion of the 2nd a-Si layer which, in effect, serves as a sacrificial etch-stop layer. A Ti layer is laid down over the **via** and allowed to thermally react with the remainder of the 2nd a-Si layer to form an elec. conductive Ti silicide region in the area of the **via** the thickness of the 2nd a-Si layer. The reaction is self-limiting and stops at the 2nd nitride layer. Subsequently a 2nd metalization layer is disposed over the **via**. Thus the partially etched 2nd a-Si layer forms a part of the 2nd metalization layer and the nitride/a-**Si**/ **nitride insulating antifuse layer** has a const. thickness detd. by the process used to lay it down, rather than on the more uncontrollable etch process. Accordingly, the programming voltage of the **antifuse** is more predictable than with prior art **antifuse** structures.

L64 ANSWER 25 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:347311 HCAPLUS
DN 122:120952
TI Semiconductor device and its manufacture
IN Jinriki, Hiroshi; Kaizuka, Kenji; Oota, Tomohiro
PA Kawasaki Steel Co, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 3

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06310687	A2	19941104	JP 1993-92960	19930420
US 5521423	A	19960528	US 1994-228257	19940415
PRAI JP 1993-90318		19930419		
JP 1993-90319		19930419		
JP 1993-92960		19930420		

AB In the title device having **antifuses**, the **insulator films** of the **antifuse** consist of a Si **film** formed by vapor deposition, and multilayers of a SiO2 **layer** and Ti, Ta, Nb, Zr, Y, Hf, or **Al oxide layer**. Alternatively, Ti, Ta, Nb, Zr, Y, and/or Hf nitride or TiB or TiC may exist between the 1st metal **layer** and the **insulator films** of the **antifuse**. The title manuf. involves the following steps: (1) forming **insulator films** on the 1st metal wiring, (2) opening a contact-**hole**, (3) depositing an **amorphous Si** on the **insulator films** by decompg. SiH4 gas with a high frequency at a low pressure, (4) depositing a metal **oxide film** by thermally decompg.

Ti, Ta, Nb, Zr, Y, or Hf alkoxide steam in an oxidizing atm. at a low pressure to form SiO2 **film** between the **amorphous** **Si** and the metal **oxide film**, and (5) forming the 2nd metal wiring.

L64 ANSWER 26 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:660663 HCAPLUS
DN 119:260663
TI Programmable ROM **anti-fuse** semiconductor devices and fabrication thereof
IN Myajima, Motomori
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05090527	A2	19930409	JP 1991-249232	19910927

AB The title device employs an amorphous Si semiconductor layer which is formed only in its through-**hole** connecting between an upper and lower circuit layers. The title amorphous **Sin** layer formed only in the through **hole** and not on the interlayer **insulator** **film** gives its step height decreased

L64 ANSWER 27 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:572182 HCAPLUS
DN 119:172182
TI Manufacture of **antifuse** region-contg. semiconductor device
IN Ootsuki, Masaya
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05121556	A2	19930518	JP 1991-281790	19911029

AB The device is manufd. by: (1) forming an elec. **insulating** **film** on a 1st elec. conducting **layer**; (2) forming a contact-**hole** to reach the conducting **layer**; (3) forming a 2nd elec. conducting **layer**; (4) patterning the 2nd conducting **layer** to remove except in the **hole**; (5) implanting impurity ion into the 2nd conducting **layer** in the **hole** for an **antifuse** region to give an amorphous **layer**; and (6) forming a 3rd elec. conducting **layer** on the 2nd conducting **layer** and the amorphous **layer**. Implantation may be done before patterning. The 2nd conducting **layer** showed good contact for the 3rd conducting **layer**

L64 ANSWER 28 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:572181 HCAPLUS
DN 119:172181
TI Manufacture of antifuse region-contg. electric circuit and programmable read only memory (PROM)
IN Tsuzuki, Norihisa
PA Fujitsu Ltd, Japan

SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 05121555	A2	19930518	JP 1991-181105	19910722

AB The circuit and PROM is manufd. by depositing a 1st elec. **insulating film** on an elec. conducting substrate, forming a **hole** to reach the substrate, forming an **amorphous Si layer** near the **hole**, depositing a **Pt layer**, reacting the Si **layer** and the **Pt layer** to form a **Pt** silicide **layer**, removing the unreacted **Pt layer**, depositing a 2nd elec. **insulating film**, and forming a contact-**hole** to reach the silicide **layer**. Over-etching of the **amorphous Si layer** was prevented.

L64 ANSWER 29 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:572179 HCAPLUS
DN 119:172179
TI Manufacture of **antifuse** region-contg. semiconductor device
IN Fujiwara, Yukio
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 05121552	A2	19930518	JP 1991-278013	19911024

AB The device is manufd. by forming a lower wiring on a substrate, forming an interlayer **insulating film**, patterning the **insulating film** for removal, forming a contact-**hole**, forming an **amorphous Si layer** in the **hole** for an **antifuse** region, oxidizing the Si **layer** to form a **Si oxide film**, irradiating with inert gas ion to remove deposits in the **hole** and the **oxide film** except the **antifuse** region, and forming an upper wiring on the **insulating film**. The **amorphous Si layer** had low defects.

L64 ANSWER 30 OF 30 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:572167 HCAPLUS
DN 119:172167
TI Manufacture of an **anti-fuse** semiconductor device
IN Fujiwara, Yukio
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI JP 05114651 A2 19930507 JP 1991-275685 19911023

AB The device is manufd. by forming an underlayer wiring on a substrate, forming an interlayer **insulating film**, patterning the **insulating film** to remove and form a contact-**hole**, forming an **amorphous Si layer** on the **insulating film**, etching the Si **layer** except for an **anti-fuse** region to reduce the thickness of the Si **layer** and form an **amorphous Si** thin **film**, irradiating with inert gas ion to remove the **amorphous Si**, and forming an upper wiring on the **insulating film**. The device showed good step coverage.

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         (c) 2001 The HW Wilson Co.
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         (c) 2001 AIAA
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         (c) 2002 INIST/CNRS
  File 238:Abs. in New Tech & Eng.  1981-2001/Dec
         (c) 2001 Reed-Elsevier (UK) Ltd.
  File 305:Analytical Abstracts  1980-2002/Dec W5
         (c) 2002 Royal Soc Chemistry
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See HELP NEWS 305.
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         (c) 2001 DECHEMA
  File  14:Mechanical Engineering Abs  1973-2002/Jan
         (c) 2002 Cambridge Sci Abs
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S3       2045   CI=(SI SS(S) N SS(S) O SS) (S) NE=3
S4     189712   SILICON(W)OXIDE OR SI(W)OXIDE OR SIO OR (OXOSILYLENE(W)28SI
              ) OR (SILICON (N) MONOXIDE) OR (SILICON(2N) MONOXIDE)
S5     105043   SILICON(W)NITRIDE OR SI(W)NITRIDE OR SIN OR (SILICON(2N) M-
             ONONITRIDE)
S6       5427   (SILICON (N)NITRIDE(N)OXIDE) OR (SILICON (N)NITRIDE(N) OX-
             IDE) OR (DISILICON(N) OXYDINITRIDE) OR (DISILICON(N) OXYNITRI-
             DE)  OR (SILICON(N)OXYNITRIDE) OR (SI(N) OXYNITRIDE? ?)
S7     132271   DIAMOND OR (DIAMOND(3N)CARBON)
S8       1124   (FLUORIN?)(W) (DOP?)(W) (OXIDE?) OR (FLUORIN?) (2N)(OXIDES)
S9       1026   F(W)DOP???
S10      1289   (ANTI(2W)FUSE? ?) OR ANTIFUSE? ? OR OTP OR ((ONE)(N)(TIME)-
             (N)(PROGRAM?))
S11    375051   (DIELECTRIC? OR OXIDE OR INSULAT?)(3N)(FILM? ? OR LAYER? OR
              COAT???? OR MATERIAL?)
S12   1141588   ((ANTI(N)REFLECT?) (2N)(COAT???? OR FILM? ? OR LAYER?)) OR
             ((DICHROIC) (2N)(FILTER? OR MIRROR)) OR (FRESNEL(W)REFLECT?) -
             OR REFLECT?
S13     93494   (POLYIMIDE? ? OR POLYAMIDE? ? OR PARYLENE OR PARALYENE)
S14   2636003   (ALUMINUM OR AL OR TUNGSTEN OR W)
S15   2780510   (COPPER OR CU OR CHROMIUM OR CR OR GOLD OR AU)
S16    620083   (PLATINUM OR PT OR PALLADIUM OR PD)
S17    692537   (SELENIUM OR SE OR GERMANIUM OR GE)
S18      2116   S8 OR S9
S19        73   S10 AND S11
S20        12   S19 AND (VIAS OR VIA OR TRENCH? OR HOLE? ? OR CHANNEL OR G-
             ROOVE? OR EDGE? OR FLUSH?)
S21        33   S19 AND (S1 OR S2 OR S4 OR S5 OR S7 OR S18)
S22         0   S19 AND (S13 OR POLYMETHYLMETHACRYLATE)
S23        36   S19 AND (S13 OR S14 OR S15 OR S16)
S24    107468   AMORPHOUS(2N)(SI OR SILICON OR C OR CARBON)
S25         9   S19 AND (S24 OR S17 OR COMPOUND(W)SEMICONDUCTOR? ? OR CERA-
             MIC? ? OR S12 OR S6 OR S3)
S26         0   S20 AND S21 AND S23 AND S25
S27         0   S21 AND S23 AND S25
S28        25   S21 AND S23
S29        44   S21 OR S23
S30        31   RD (unique items)
S31        41   S30 OR S20 OR S25
S32        38   RD (unique items)
S33        38   S32 NOT PD>=20010604
```

? T S33/3,AB/1-38

>>>No matching display code(s) found in file(s): 65

33/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6747320 INSPEC Abstract Number: B2000-12-2530G-001
Title: Breakdown mechanism of **Al**/sub 2/O/sub 3/ based metal-to-metal **antifuses**
Author(s): Wei-Tang Li; McKenzie, D.R.; McFall, W.D.; Qi-Chu Zhang; Wiszniewski, W.
Author Affiliation: Dept. of Appl. Phys., Sydney Univ., NSW, Australia
Journal: Solid-State Electronics vol.44, no.9 p.1557-62
Publisher: Elsevier,
Publication Date: Sept. 2000 Country of Publication: UK
CODEN: SSELA5 ISSN: 0038-1101
SICI: 0038-1101(200009)44:9L.1557:BMAB;1-Z
Material Identity Number: S068-2000-009
U.S. Copyright Clearance Center Code: 0038-1101/2000/$20.00
Language: English
Abstract: An impulse thermal breakdown model is proposed to understand the breakdown mechanism of **Al** /sub 2/O/sub 3/ thin film based metal-to-metal **antifuses** . In this model, the electric field dependence as well as the temperature dependence of the electrical conductivity is considered. The I-V characteristic of the **antifuses** indicated that the conductivity of **Al**/sub 2/O/sub 3/ rose greatly under high field. The threshold breakdown voltage of the **antifuses** was shown by experiment to be proportional to its insulator thickness and to the square root of the insulator resistivity. When breakdown of the **antifuses** was carried out by applying constant voltage pulse, the inverse square root of the time to breakdown was shown to be proportional to the amplitude of the pulse. All the experimental results were found to be consistent with the theoretical results of the model. In addition, an **antifuse** breakdown filament with a diameter of 150 nm was observed by using a scanning electron microscope.
Subfile: B

33/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6260720 INSPEC Abstract Number: B1999-07-2530G-001
Title: Effect of different barrier materials on **antifuse** performance
Author(s): Ang, T.C.; Tse, M.S.; Chan, L.; Sudijono, J.L.
Author Affiliation: Sch. of Electr. & Electron. Eng., Nanyang Technol. Inst., Singapore
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3510 p.233-9
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1998 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1998)3510L.233:EDBM;1-#
Material Identity Number: C574-1998-269
U.S. Copyright Clearance Center Code: 0277-786X/98/$10.00

Conference Title: Microelectronic Manufacturing Yield, Reliability, and Failure Analysis IV
Conference Sponsor: SPIE
Conference Date: 23-24 Sept. 1998 Conference Location: Santa Clara, CA, USA
Language: English
Abstract: An **antifuse** is a programmable interconnect element used in field programmable gate arrays (FPGAs). It is made up of an **insulating layer** sandwiched by 2 electrodes. The device is normally off and has a high resistance when unprogrammed. However, with the application of a programming voltage or current pulse, the **antifuse** turns into a `fuse' of low resistance due to the breakdown of the insulator, accompanied by the formation of a conductive path or filament through the **insulating layer**. Metal to metal **antifuses** are favored for high speed and high density FPGAs because they offer low on-resistance, small device area and high reliability. In FPGAs incorporating **antifuses**, there are typically thousands of **antifuses** and their leakage currents are quite substantial, thereby leading to considerable power consumption. Leakage current, I/sub leakage/ reduction can be achieved through the discerning choice of electrodes, **antifuse** stack material, stack composition, thickness and film deposition process conditions amongst others. In this paper, the electrical characteristics of the **amorphous silicon**-based **antifuse** with different types of barrier layers are presented. We show that the inclusion of an in-situ top barrier layer in the a-Si:H based **antifuse** leads to a significant reduction in the leakage current with no appreciable increase in the programming voltage.
Subfile: B

33/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6194619 INSPEC Abstract Number: B1999-04-2190-001
Title: Metal-to-metal **antifuse** with amorphous Ti-rich barium titanate **film** and **silicon oxide film**
Author(s): Jae Sung Lee; Young Hyun Lee
Author Affiliation: Dept. of Comput. & Commun. Eng., Uiduk Univ., Kyongbuk, South Korea
Journal: Solid-State Electronics vol.43, no.3 p.469-72
Publisher: Elsevier,
Publication Date: March 1999 Country of Publication: UK
CODEN: SSELA5 ISSN: 0038-1101
SICI: 0038-1101(199903)43:3L.469:MMAW;1-4
Material Identity Number: S068-1999-001
U.S. Copyright Clearance Center Code: 0038-1101/99/$20.00
Language: English
Abstract: This paper is focused on the fabrication of reliable novel **antifuse** , which could operate at low voltage along with the improvement in off and on-state properties. An **antifuse** composed of Ti-rich barium titanate/**silicon oxide** sandwiched between **Al** and TiW-silicide has been developed for high reliable field programmable devices. The breakdown voltage of an **antifuse** is properly reduced by using amorphous Ti-rich barium titanate film and leakage current is not significantly increased due to the high quality of **silicon oxide** . Low on-resistance (46 Omega / mu m/sup 2/) and low programming voltage (9 V) is demonstrated in these **antifuses** with

a 220 AA double **insulator layer** while keeping sufficient off-state reliability. A significant capacitance reduction at high operating frequencies is also realized.
Subfile: B

33/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6064678 INSPEC Abstract Number: B9812-1265B-020
Title: **Antifuse** with Ti-rich barium titanate **film** and **silicon oxide film**
Author(s): Lee, J.S.; Lee, Y.H.
Journal: Journal of the Institute of Electronics Engineers of Korea D vol.35-D, no.7 p.72-8
Publisher: Inst. Electron. Eng. Korea,
Publication Date: July 1998 Country of Publication: South Korea
CODEN: CKODF8 ISSN: 1226-5845
SICI: 1226-5845(199807)35D:7L.72:AWRB;1-B
Material Identity Number: G412-98008
Language: Korean
Abstract: This paper is focused on the fabrication of a reliable novel **antifuse** , which could operate at low voltage and provide an improvement in OFF and ON-state properties in an FPGA. The fabricated **antifuse** consists of a **Al**-BaTi/sub 2/O/sub 3/-**SiO**/sub 2/-TiW-silicide structure. Through systematic analyses for bottom metal and the intermetallic **insulator**, **material** and electrical properties were investigated. TiW-silicide as the bottom electrode had a smooth surface with average roughness of 11 AA at 10*10 mu m/sup 2/ and kept the as-deposited **SiO** /sub 2/ film stable. The amorphous BaTi/sub 2/O/sub 3/ film was chosen as the other insulator because of its low breakdown strength (2.5 MV/cm). The breakdown voltage of the **antifuse** is remarkably reduced by using a BaTi/sub 2/O/sub 3/ film, and leakage current is maintained at that low level due to the **SiO**/sub 2/ film. Low ON-resistance (46 Omega / mu m/sup 2/) and low programming voltage (9.1 V) can be obtained in these **antifuses** with a 220 AA double **insulator layer** and 19.6*10/sup -6/cm/sup 2/ area, while keeping sufficient OFF-state reliability (less than 1 nA).
Subfile: B

33/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5452319 INSPEC Abstract Number: B9702-2530G-001
Title: High performance **antifuse** with planar double dielectrics on Si/sub 1-x/**Ge** /sub x/ pad for field programmable gate array applications
Author(s): Kim, J.; Park, M.Y.; Song, Y.H.; Baek, J.T.
Author Affiliation: Semicond. Div., Electron. & Telecommun. Res. Inst., Taejon, South Korea
Journal: Electronics Letters vol.32, no.24 p.2276-7
Publisher: IEE,
Publication Date: 21 Nov. 1996 Country of Publication: UK
CODEN: ELLEAK ISSN: 0013-5194

SICI: 0013-5194(19961121)32:24L.2276:HPAW;1-C
Material Identity Number: E089-96024
U.S. Copyright Clearance Center Code: 0013-5194/96/$10.00
Language: English
Abstract: A new **antifuse** device with a planar metal/dielectric/poly-Si/sub 1-x/**Ge**/sub x//dielectric/metal structure has been proposed for use in FPGAs as a voltage programmable link. The device has low leakage current (~0.01 pA/**antifuse**) at an operating voltage of 5 V and low on-resistance (~13-15 Omega) with a 1 ms long 12.5 V pulse.
Subfile: B

33/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5447917 INSPEC Abstract Number: B9701-2550F-038
Title: Device characteristics and metal link formation in the planar **antifuse** with poly-Si pad
Author(s): Baek, J.T.; Jung, S.H.; Kang, S.W.; Ahn, B.T.
Author Affiliation: Dept. of Mater. Sci. & Eng., Korea Adv. Inst. of Sci. & Technol., Seoul, South Korea
Journal: Journal of the Korean Institute of Telematics and Electronics vol.33A, no.8 p.158-66
Publisher: Korea Inst. Telematics & Electron,
Publication Date: Aug. 1996 Country of Publication: South Korea
CODEN: CKNOEZ ISSN: 1016-135X
SICI: 1016-135X(199608)33A:8L.158:DCML;1-J
Material Identity Number: N523-96024
Language: Korean
Abstract: The programming phenomena of an **antifuse** device with a planar **Al**-**SiO**/sub 2/-polysilicon-**SiO**/sub 2/-**Al** structure were investigated using a parameter analyzer, an optical microscope and a scanning electron microscope. When the breakdown voltage was applied, one or two **holes** were formed on the **SiO**/sub 2/ **layer** by **oxide** breakdown and **Al** flowed through the **holes** into the poly Si layer. With further application of voltage after breakdown, **Al** from the positive electrode flowed into the poly-Si layer and the two electrodes were connected by AlSi alloy. The resistances of the device before and after oxide breakdown were a few G Omega and about 1 k Omega , respectively. Furthermore, the resistance drastically reduced to nearly 30 Omega after forming the AlSi conducting line between the two electrodes. The conducting line between the two electrodes grew a few cm/sec when the applied voltage was above the critical voltage. The critical voltage was proportional to the length of devices, indicating that critical current exists. The measured critical current was about 8 mA when the width of the device was 2.4 mu m. It is supposed that the polysilicon in front of the conducting line was partially melted by Joule heating caused by current crowding, and fast growth of the conducting line was possible.
Subfile: B

33/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

5345383 INSPEC Abstract Number: B9609-2550F-039
Title: The interfacial properties of the annealed **SiO**/sub 2/-TiW structure
Author(s): Jae Sung Lee; Hyung Ho Park; Jung Hee Lee; Yong Hyun Lee
Author Affiliation: Dept. of Electr. Eng., Kyungpook Nat. Univ., Taegu, South Korea
Journal: Journal of the Korean Institute of Telematics and Electronics vol.33A, no.3 p.117-25
Publisher: Korea Inst. Telematics & Electron,
Publication Date: March 1996 Country of Publication: South Korea
CODEN: CKNOEZ ISSN: 1016-135X
SICI: 1016-135X(199603)33A:3L.117:IPAS;1-0
Material Identity Number: N523-96014
Language: Korean
Abstract: The variation of the interfacial and the electrical properties of **SiO** /sub 2/-TiW layers as a function of anneal temperature was extensively investigated. During the deposition of **SiO**/sub 2/ on TiW, chemical bonds such as **SiO**/sub 2/, TiW, WO/sub 3/, WO/sub 2/, TiO/sub 2/, Ti/sub 2/O/sub 3/ and/or Ti/sub 3/O/sub 5/ were created at the **SiO**/sub 2/-TiW interface. At the anneal temperature of 300 degrees C, WO/sub 3/ and TiO/sub 2/ bonds began to break due to the reduction phenomena of **W** and Ti, and simultaneously metallic **W** and Ti bonds started to create. Above 500 degrees C, part of the Si-O bonds were broken, and consequently Ti/**W** silicide was formed. From the current-voltage characteristics of the **Al-SiO** /sub 2/ (220 AA)-TiW **antifuse** structure, it was found that the breakdown voltage of the **antifuse** device decreased with increasing annealing temperature for the **SiO**/sub 2/ (220 AA)-TiW **layer**, when the **insulating** properties of the **antifuse** device were affected by the deterioration of the intermetallic **SiO**/sub 2/ film caused by the inflow of Ti and **W**.
Subfile: B

33/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

5264116 INSPEC Abstract Number: B9606-2190-001
Title: Extremely low ON-resistance metal-to-metal **antifuses** with **Al-Cu**/10 nm-thick p-**SiN**/sub x//**Al-Cu** structure for next generation very high speed FPGAs (field programmable gate arrays)
Author(s): Tamura, Y.; Kimura, Y.; Tsutsui, C.; Shinriki, H.
Author Affiliation: Adv. Technol. Res. Section, Kawasaki Steel Corp., Chiba, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes (Japan) vol.35, no.2B p.1049-53
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: Feb. 1996 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199602)35:2BL.1049:ERMM;1-X
Material Identity Number: C579-96005
Conference Title: 1995 International Conference on Solid State Devices and Materials (SSDM `95)
Conference Date: 21-24 Aug. 1995 Conference Location: Osaka, Japan

Language: English
Abstract: We present a novel metal-to-metal **antifuse** structure consisting of a plasma enhanced CVD (chemical vapor deposition) **silicon nitride** (p-**SiN**/sub x/) **dielectric film** sandwiched between two **aluminum** layers. The leakage current in the off-state is markedly reduced by using **aluminum** film as the upper electrode instead of Ti(titanium) or TiN(titanium nitride) film. A **Al-Cu**/10 nm-thick p-**SiN**/sub x//**Al-Cu** structure **antifuse** provides sufficient long-term off-state reliability exceeding ten years at 3.6 V while keeping low breakdown voltage (10 V). An extremely low on-resistance of around 3 Omega and a narrow distribution are also realized. A new **antifuse** structure (**Al-Cu**/p-**SiN**/sub x//**Al-Cu**(100 nm)/Ti/TiN/ **Al-Cu**) highly compatible with the conventional **via** formation process in double metal interconnect wiring is proposed. This type of **antifuse** structure is very promising for next-generation very high-speed FPGAs.
Subfile: B

33/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

5165891 INSPEC Abstract Number: A9604-6848-004, B9603-2530G-001
Title: Interfacial reaction in the sputter-deposited **SiO** /sub 2//Ti/sub 0.1/**W**/sub 0.9/ **antifuse** system
Author(s): Jong Tae Baek; Hyung-Ho Park; Kyung-Ik Cho; Hyung Joun Yoo; Sang Won Kang; Byung Tae Ahn
Author Affiliation: Semicond. Technol. Div., Electron. & Telecommun. Res. Inst., Taejon, South Korea
Journal: Journal of Applied Physics vol.78, no.12 p.7074-9
Publisher: AIP,
Publication Date: 15 Dec. 1995 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(19951215)78:12L.7074:IRSD;1-K
Material Identity Number: J004-96001
U.S. Copyright Clearance Center Code: 0021-8979/95/78(12)/7074/6/$6.00
Language: English
Abstract: The effects of annealing temperature on the interfacial reactions and the **antifuse** I-V characteristics of ultra thin **SiO**/sub 2/ layer deposited on Ti/sub 0.1/**W**/sub 0.9/ substrate were investigated. The interfacial reactions were analyzed using X-ray photoelectron spectroscopy and Auger electron spectroscopy with the sample which is in situ annealed under ultra high vacuum or ex situ annealed in a nitrogen atmosphere. The surface of the Ti/sub 0.1/**W** /sub 0.9/substrate was oxidized during sputter deposition of **SiO**/sub 2/ layer. Ti, **W** oxides consist of Ti/sub 2/O/sub 3/(Ti/sub 3/O/sub 5/), TiO/sub 2/, WO/sub 2/, and WO/sub 3/. The WO/sub 3/ and Ti/sub 2/O/sub 3/ decomposed into metallic **W** and Ti at 400 and 500 degrees C, respectively. The breakdown voltage of the **antifuse** decreased as the annealing temperature increased, due to the thinning of the **dielectric layer** resulting from the decomposition of Ti; **W** oxides and the formation of metallic **W** and Ti. Annealing at 600 degrees C caused the reaction between metallic (Ti,**W**) and the **SiO**/sub 2/ layer and formed elemental silicon in the **dielectric layer**, where the **SiO**/sub 2/ **layer** completely lost its **dielectric** property the breakdown of dielectric property might form a

metallic **channel** in the **SiO**/sub 2/ film, which mainly contains metallic **W**, Ti, and Si.
Subfile: A B

33/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

5090856 INSPEC Abstract Number: B9512-2570-012
Title: Ultra clean processing for ULSI
Author(s): Ohmi, T.
Author Affiliation: Dept. of Electron., Tohoku Univ., Sendai, Japan
Journal: Microelectronics Journal vol.26, no.6 p.595-619
Publication Date: Sept. 1995 Country of Publication: UK
CODEN: MICEB9 ISSN: 0026-2692
U.S. Copyright Clearance Center Code: 0026-2692/95/$9.50
Language: English
Abstract: The simultaneous fulfilment of three principles, viz. ultraclean water surface, ultra-clean processing environment, and perfect process-parameter control, is the key to high-performance fabrication of advanced subhalf-micron and subquarter-micron ULSI devices. The importance of this ultra-clean processing concept is demonstrated by the experimental results of low-temperature silicon epitaxy by low-kinetic-energy Ar ion bombardment. By optimizing process parameters under ultra-clean conditions, high-crystallinity silicon epitaxial layers are successfully grown at temperatures as low as 250 degrees C, with accompanying simultaneous doping. Advanced **copper** metallization for large-current driving interconnect is also achieved. Giant-grain **copper** thin films, also formed by low-kinetic-energy Ar ion bombardment, exhibit very low resistivity and excellent reliability against electromigration and stress migration. Native and chemical-oxide-free processing produces ideal metal-to-silicon contacts with very low resistance, i.e. 10/sup -9/ Omega .cm/sup 2/. Ultra-clean-hydrogen-radical-balanced and surface-microroughnes s-free-oxidation is confirmed to form high quality, very thin **oxide films** of 5 to 10 nm, with complete uniformity and very strong resistance to hot electron injection. Low-temperature annealing ion implantation makes practical a metal gate self-aligned MOS LSI, which is crucial for high current driving capability in high-speed CMOS. All of these advanced fabrication technologies, realized for the first time by ultraclean techniques, allow total low-temperature processing, such as gate oxidation at 450 degrees C, implanted region annealing at 450 degrees C and single-crystal silicon epitaxy at 300 degrees C, which is essential for high-performance subhalf-micron and subquarter-micron ULSI. **Oxide layer** -free metal-to-silicon and metal-to-metal film deposition is freely available in ultra-clean processes, so that field-programmable **anti-fuse** technology is achievable by current drive silicidation as well as by very low resistance metal/silicon and metal/metal contact.
Subfile: B

33/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

4941924 INSPEC Abstract Number: B9506-2530G-003

Title: Relation between stress-induced leakage current and dielectric breakdown in **SiN**-based **antifuses**
Author(s): Yasuda, H.; Ikeda, N.; Hama, K.; Takagi, M.T.; Yoshii, I.
Author Affiliation: Semicond. Device Eng. Lab., Toshiba Corp., Kawasaki, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) vol.34, no.3 p.1488-92
Publication Date: March 1995 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
Language: English
Abstract: We report on the degradation process of metal-to-metal **antifuses** that use thin **silicon nitride film** as the **dielectric layer** under high electric held stress. Stress-induced leakage current was observed in all samples, and it flows through local spots. Two-level fluctuations were found on the leakage current well below the stress voltage, and large and complex fluctuations were observed near the stress voltage. The conduction mechanism of the stress-induced leakage current was the Poole-Frenkel type. It was found that the dielectric constant of the path became large and that the breakdown and the anomalous current depended on the barrier metal thickness. Considering these results, the stress-induced leakage current and the breakdown are thought to be caused by electromigration of electrode material to the **SiN** film.
Subfile: B

33/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

4886259 INSPEC Abstract Number: B9504-1265B-042
Title: Most promising metal-to-metal **antifuse** based 10 nm-thick p-**SiN**/sub x/ film for high density and high speed FPGA application
Author(s): Tamura, Y.; Shinriki, H.
Author Affiliation: LSI Res. Lab., Kawasaki Steel Corp., Chiba, Japan
p.285-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA 947 pp.
ISBN: 0 7803 2111 1
U.S. Copyright Clearance Center Code: 0 7803 2111 1/94/$4.00
Conference Title: Proceedings of 1994 IEEE International Electron Devices Meeting
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 11-14 Dec. 1994 Conference Location: San Francisco, CA, USA
Language: English
Abstract: A novel metal-to-metal **antifuse** has been developed for highly reliable and high performance 3.3 V operated FPGAs. Dielectric breakdown reliability is remarkably improved by using amorphous-like WSi/sub x/ film as a bottom electrode having extremely smooth surface. Sufficient low ON-resistance (8.2 Omega) and low programming voltage (9 V) can be also obtained in the metal-to-metal **antifuses** having WSi/sub x//**SiN**/sub x/(10 nm)/TiN structure while keeping sufficient OFF-state reliability. By using WSi/sub x//**SiN**/sub x//**Al-Cu** structure, lowest ON-resistance (2 Omega) can be obtained. These metal-to-metal **antifuse** structures are very promising for next generation FPGAs.
Subfile: B

33/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

4767690 INSPEC Abstract Number: B9411-2530N-001
Title: Metal-to-metal **antifuses** with very thin silicon dioxide films
Author(s): Zhang, G.; Hu, E.; Yu, P.; Chiang, S.; Hamdy, E.
Author Affiliation: Dept. of Phys., California Univ., Berkeley, CA, USA
Journal: IEEE Electron Device Letters vol.15, no.8 p.310-12
Publication Date: Aug. 1994 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/94/$04.00
Language: English
Abstract: **Antifuse** samples with very thin insulating oxide were fabricated using a technique of two-step PECVD oxide deposition. Dielectric strength as high as 13 MV/cm was obtained for our samples. Defect density and uniformity have been improved in this way. The on-state resistance of the programmed **antifuses** shows a stronger dependence on the oxide thickness when it was programmed at the lower current than when it was programmed at the higher current.
Subfile: B

33/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

04353413 INSPEC Abstract Number: B9304-2550E-027
Title: Conductive **channel** in ONO formed by controlled dielectric breakdown
Author(s): Chiang, S.; Wang, R.; Speers, T.; McCollum, J.; Hamdy, E.; Hu, C.
Author Affiliation: Actel Corp., Sunnyvale, CA, USA
Conference Title: 1992 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.92CH3172-4) p.20-1
Publisher: IEEE, New York, NY, USA
Publication Date: 1992 Country of Publication: USA x+120 pp.
ISBN: 0 7803 0698 8
U.S. Copyright Clearance Center Code: 92CH3172-4/92/0000-0020$03.00
Conference Sponsor: IEEE; Japan Soc. Appl. Phys
Conference Date: 2-4 June 1992 Conference Location: Seattle, WA, USA
Language: English
Abstract: Cross-section TEM photos that capture the conductive **channel** of **oxide**-nitride-**oxide** (ONO) **films** after electric breakdown are discussed. The photos reveal a single crystal or polycrystal **channel** with a dome-shaped cap depending on the breakdown current. The implications of this structure for electric characteristics is analyzed with a spherical thermal-electric model. When ONO films are used as **antifuse** on FPGA product, the resistance of the **antifuse** can be controlled by choosing a sufficiently large programming current level and the resistance remains stable during 1000 h of burn-in at 125 degrees C and 5.75 V. Negligible change in delay time along many different data paths was observed.
Subfile: B

33/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

04271689 INSPEC Abstract Number: B9212-1265B-093, C9212-5140-001
Title: Actel locate the **antifuse** dielectric
Author(s): Flaherty, N.; Neale, R.
Journal: Electronic Engineering vol.64, no.789 p.41-2, 44, 47
Publication Date: Sept. 1992 Country of Publication: UK
CODEN: ELCEA9 ISSN: 0013-4902
Language: English
Abstract: Actel have recently released the first side elevation TEMs of programmed ONO (oxide-nitride-oxide) **antifuses** of the type used in their family of FPGAs. These new micrographs finally determine the critical post programming location of the dielectric and throw new light on the programming mechanism. The authors explore the new evidence and critically review its interpretation.
Subfile: B C

33/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

03910659 INSPEC Abstract Number: B91043851, C91041202
Title: A reflow model for the **anti-fuse**
Author(s): Neale, R.
Journal: Electronic Engineering vol.63, no.772 p.31-2, 35-6, 38, 40
Publication Date: April 1991 Country of Publication: UK
CODEN: ELCEA9 ISSN: 0013-4902
Language: English
Abstract: From an investigation that started in response to questions regarding the safety of some of the reliability conclusions drawn with respect to the **anti-fuse** element used in PLDS the author proposes a new and elegant model for the operation of the device, that if fully verified will clear any reliability doubts. A number of different material compositions are used by different manufacturers. They all have the basic metal-thin **film dielectric**-metal sandwich structure. The dielectric is usually silica (**SiO**/sub 2/) or a layered silica-**silicon nitride** -silica sandwich composite, other dielectrics such as **amorphous silicon** are also used. Here devices with dielectrics of a thickness of the order of 100 AA are considered. In operation the application of a voltage of the order 10-20 V results in dielectric breakdown and the establishment of a permanent conducting link with a resistance of from 300 to 1000 Omega . It is that link that is then used to selectively couple the logic elements of the circuit.
Subfile: B C

33/3,AB/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

03809770 INSPEC Abstract Number: B91008213
Title: Oxide-nitride-oxide **antifuse** reliability
Author(s): Chiang, S.; Wang, R.; Chen, J.; Hayes, K.; McCollum, J.; Hamdy, E.; Hu, C.
Author Affiliation: Actel Corp., Sunnyvale, CA, USA
Conference Title: 28th Annual Proceedings. Reliability Physics 1990 (Cat.

No.90CH2787-0) p.186-92
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA vi+322 pp.
U.S. Copyright Clearance Center Code: CH2787-0/90/0000-0186$01.00
Conference Sponsor: IEEE
Conference Date: 27-29 March 1990 Conference Location: New Orleans, LA, USA
Language: English
Abstract: Compact, low-resistance oxide-nitride-oxide (ONO) **antifuses** are studied for time-dependent dielectric breakdown (TDDB), program disturb, programmed **antifuse** resistance stability, and effective screen. ONO **antifuses** are superior to oxide **antifuses** . No ONO **antifuse** failures were observed in 1.8 million accelerated burn-in device-hours accumulated on 1108 product units. This is in agreement with the 1/E field acceleration model.
Subfile: B

33/3,AB/18 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05792125
E.I. No: EIP01025548923
Title: Scalability study of laser-induced vertical make-link structure
Author: Lee, Joo-Han; Zhang, Wei; Bernstein, Joseph B.
Corporate Source: Univ of Maryland at College Park, College Park, MD, USA
Source: IEEE Transactions on Semiconductor Manufacturing v 13 n 4 Nov 2000. p 442-447
Publication Year: 2000
CODEN: ITSMED ISSN: 0894-6507
Language: English
Abstract: The scalability of a direct metal-to-metal connection between two different levels of metallizations has been extrapolated to be compatible with modern semiconductor fabrication technology. A simple equation to evaluate the scalability was formulated based on focused ion beam (FIB) cross-sectional images of larger link structures with various sizes. With a 0.6- mu m-thick metal 1 line and a 0.5- mu m-thick interlevel dielectric (ILD), a width of less than 0.5 mu m is evaluated to be possible for the metal 1 line. Two limitations exist in the process of scaled-down link structures, which are the ratio of the thickness of ILD to the thickness of the metal 1 line, t//I//L//D/t//m, and the quality of laser beam parameters including the spot size and positioning error. However, modern processing technologies and advanced laser processing systems are considered to allow the scalability of a vertical make-link structure. Two layouts of two-level interconnects were designed with increased interconnect densities with a 1- mu m pitch of a 0.5- mu m-wide metal 1 line. These results demonstrate the application of commercially viable vertical linking technology to very large-scale integration (VLSI) applications. (Author abstract) 13 Refs.

33/3,AB/19 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05265460
E.I. No: EIP99034606637
Title: Metal-to-metal **antifuse** with amorphous Ti-rich barium

titanate **film** and **silicon oxide film**
Author: Lee, Jae Sung; Lee, Young Hyun
Corporate Source: Uiduk Univ, Kyongbuk-do, South Korea
Source: Solid-State Electronics:An International Journal v 43 n 3 Mar 1999. p 469-472
Publication Year: 1999
CODEN: SSELA5 ISSN: 0038-1101
Language: English
Abstract: This paper is focused on the fabrication of reliable novel **antifuse**, which could operate at low voltage along with the improvement in off and on-state properties. An **antifuse** composed of Ti-rich barium titanate/**silicon oxide** sandwiched between **Al** and TiW-silicide has been developed for high reliable field programmable devices. The breakdown voltage of an **antifuse** is properly reduced by using amorphous Ti-rich barium titanate film and leakage current is not significantly increased due to the high quality of **silicon oxide**. Low on-resistance (46 Omega / mu m**2) and low programming voltage (9 V) is demonstrated in these **antifuses** with a 220 angstroms double **insulator layer** while keeping sufficient off-state reliability. A significant capacitance reduction at high operating frequencies is also realized. (Author abstract) 6 Refs.

33/3,AB/20 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05116709
E.I. No: EIP98094374243
Title: New metal-to-metal **antifuse** with **amorphous carbon**
Author: Liu, S.; Lamp, D.; Gangopadhyay, S.; Sreenivas, G.; Ang, S.S.; Naseem, H.A.
Corporate Source: Texas Tech Univ, Lubbock, TX, USA
Source: IEEE Electron Device Letters v 19 n 9 Sep 1998. p 317-319
Publication Year: 1998
CODEN: EDLEDZ ISSN: 0741-3106
Language: English
Abstract: We report the development of a new metal-to-metal **antifuse** with **amorphous carbon** as the dielectric. **Amorphous carbon antifuses** have several characteristics making them superior to **amorphous silicon antifuses**, including lower values of OFF-state leakage current, ON-state resistance, dielectric constant, and breakdown voltage. Most importantly, **amorphous carbon antifuses** do not show ON-OFF switching, which is observed in **amorphous silicon antifuses**. A new model is proposed to explain the breakdown mechanism and ON-state reliability of **amorphous carbon antifuses**. (Author abstract) 22 Refs.

33/3,AB/21 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04616394
E.I. No: EIP97023518606
Title: Investigation of link formation in a novel planar-type **antifuse** structure

Author: Baek, Jong Tae; Park, Hyung-Ho; Kang, Sang Won; Ahn, Byung Tae; Yoo, Ilyung Joun
Corporate Source: Electronics and Telecommunications Research Inst, Taejon, South Korea
Source: Thin Solid Films v 288 n 1-2 Nov 15 1996. p 41-44
Publication Year: 1996
CODEN: THSFAP
Language: English
Abstract: A novel **antifuse** structure with planar-type polysilicon pad is described. The formation of a link between the **aluminum** electrodes after application of a programming voltage was also investigated. The structure consists of **Al/SiO//2/poly-Si/ SiO//2/Al** layers. The poly-Si pad was doped with boron and the thickness of the **antifuse** dielectric was 9 nm. When a programming voltage is applied, the electrodes are connected by the mass transfer of **aluminum** through the dielectric and the doped polysilicon pad. The on-state resistance of about 10 Omega , which is the lowest on-state resistance ever reported, is obtained after breakdown with 9.9 V programming voltage. Scanning Auger microscopy analyses show the propagation of a link, as mass transfer of **aluminum** in the boron doped polysilicon pad. The elliptical link has a maximum diameter of 1.0 mu m in the horizontal direction and a minimum diameter of 320 nm in the vertical direction. (Author abstract) 6 Refs.

33/3,AB/22 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04239896
E.I. No: EIP95092839957
Title: **Anti-fuse** developments - a pattern emerges
Author: Anon
Source: Electronic Engineering (London) v 67 n 822 Jun 1995. 3pp
Publication Year: 1995
CODEN: ELEGAP ISSN: 0013-4902
Language: English
Abstract: The IRPS-95 (International Reliability Physics Symposium) has added some more information to the developments of the **amorphous silicon**-based **anti-fuse**, the M-aSi-M type. The first is the agreed advantage of the low temperature (about 300 degree C) CVD deposition process for **amorphous silicon** as the material most suited for devices that must be deposited late in the process. The second is the confirmation that the effect of voltage stress saturate at a value that would not compromise the off-state integrity when devices are operated at 5V, the normal operating voltage. As the silicon industry in general moves to 3.3V and lower, use of the **amorphous silicon**-based **anti-fuses** is found to be highly plausible. 6 Refs.

33/3,AB/23 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04229455
E.I. No: EIP95082825068
Title: Electro-thermal model for metal-oxide-metal **antifuses**
Author: Zhang, Guobiao; Hu, Chenming; Yu, Peter Y.; Chiang, Steve; Eltoukhy, Shafy; Hamdy, Esmat Z.

Corporate Source: Univ of California, Berkeley, CA, USA
Source: IEEE Transactions on Electron Devices v 42 n 8 Aug 1995. p 1548-1558
Publication Year: 1995
CODEN: IETDAI ISSN: 0018-9383
Language: English
Abstract: In this paper, a complete electro-thermal analysis is presented for the metal-oxide-metal **antifuses**. The application of the Wiedemann-Franz Law and the thin film effect on thermal and electrical conductivities of metal films were also discussed. Several key parameters for **tungsten**-oxide-**tungsten antifuse** were extracted. The reaction temperature between **tungsten** and oxide was estimated to be around 1300 degree C. The core resistivity was found to be around 250 mu Omega center dot cm. This model can be readily extended to the other metal-dielectric-metal systems. (Author abstract) 24 Refs.

33/3,AB/24 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04209901
E.I. No: EIP95072775471
Title: ON-state, programming and OFF-state reliability of metal-to-metal **antifuse** based 10 nm-thick SiNx film for 3.3 V operation
Author: Tamura, Yoshimitsu; Shinriki, Hiroshi
Corporate Source: Kawasaki Steel Corp, Chiba, Jpn
Conference Title: Proceedings of the 33rd Annual 1995 IEEE International Reliability Physics Proceedings
Conference Location: Las Vegas, NV, USA Conference Date: 19950404-19950406
E.I. Conference No.: 43296
Source: Annual Proceedings - Reliability Physics (Symposium) 1995. IEEE, Piscataway, NJ, USA,95CH3471-0. p 36-41
Publication Year: 1995
CODEN: ARLPBI ISSN: 0099-9512
Language: English
Abstract: Reliability of newly a developed metal-to-metal **Antifuse** (**Al**-0.5**%Cu**/10 nm-thick SiNx/amorphous-like WSix) with very low ON-resistance below 10 ohm has been investigated. Sufficient OFF-state reliability can be obtained by using amorphous-like WSix film as a lower electrode, which has a remarkably smooth surface without sharp protrusions. By using **Al-Cu** film as an upper electrode, low ON-resistance can be easily obtained with a wide range of programming current down to 0.1 mA, which is enough to melt the lower portion of **Al-Cu** film and to diffuse **aluminum** into the SiNx film due to joule heating generated at filament. Moreover, favorable electromigration (EM) performance and ON-state stability of the **Antifuse** programmed in plus polarity could be obtained. The result could be attributed to the final state of the filament composed of **Al-W-Si**, which is formed by a reaction between electromigrated **tungsten** through ruptured SiNx film and locally melted **aluminum** just on the ruptured SiNx film due to joule heating. (Author abstract) 10 Refs.

33/3,AB/25 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04168604
E.I. No: EIP95052707313
Title: Most promising metal-to-metal **antifuse** based 10 nm-thick p-SiNx film for high density and high speed FPGA application
Author: Tamura, Yoshimitsu; Shinriki, Hiroshi
Corporate Source: Kawasaki Steel Corp, Chiba, Jpn
Conference Title: Proceedings of the 1994 IEEE International Electron Devices Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19941211-19941214
E.I. Conference No.: 43001
Source: Technical Digest - International Electron Devices Meeting 1994. IEEE, Piscataway, NJ, USA,94CH35706. p 285-288
Publication Year: 1994
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: A novel metal-to-metal **Antifuse** has been developed for highly reliable and high performance 3.3 V operated FPGAs. Dielectric breakdown reliability is remarkably improved by using amorphous-like WSix film as a bottom electrode having extremely smooth surface. Sufficient low ON-resistance (8.2 Omega) and low programming voltage (9 V) can be also obtained in the metal-to-metal **Antifuses** having WSix/SiNx(10 nm)/TiN structure while keeping sufficient OFF-state reliability. By using WSix/SiNx/**Al**-**Cu** structure, lowest ON-resistance (2 omega) can be obtained. These metal-to-metal **Antifuse** structures are very promising for next generation FPGAs. (Author abstract) 5 Refs.

33/3,AB/26 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03907150
E.I. No: EIP94061318350
Title: Highly reliable metal-to-metal **antifuse** for high-speed field programmable gate arrays
Author: Takagi, Mariko; Yoshii, Ichiro; Ikeda, Naoki; Yasuda, Hiroaki; Hama, Kaoru
Corporate Source: Toshiba Corp, Kawasaki, Jpn
Conference Title: Proceedings of the 1993 IEEE International Electron Devices Meeting
Conference Location: Washington, DC, USA Conference Date: 19931205-19931208
E.I. Conference No.: 20137
Source: Technical Digest - International Electron Devices Meeting 1993. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p 31-34
Publication Year: 1993
CODEN: TDIMD5 ISSN: 0163-1918 ISBN: 0-7803-1450-6
Language: English
Abstract: This paper describes a novel metal-to-metal **antifuse** technology for field programmable gate arrays which achieves very high performance and reliability while maintaining full CMOS compatibility. Plasma-CVD **SiN** with Si-N equals 1 and **Al** covered with TiN are used as an **antifuse** dielectric and electrodes, respectively. This structure allows a desirable characteristics for high-speed FPGAs with off-state reliability of 1.7 multiplied by 10**5 years. (Author abstract) 5 Refs.

33/3,AB/27 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03409511
E.I. Monthly No: EI9204049261
Title: A sublithographic **antifuse** structure for field-programmable gate array applications.
Author: Chen, Kueing-Long; Liu, David K. Y.; Misium, George; Gosney, W. Milton; Wang, Shoue-Jen; Camp, Janet; Tigelaar, Howard
Corporate Source: Texas Instruments Inc, Dallas, TX, USA
Source: IEEE Electron Device Letters v 13 n 1 Jan 1992 p 53-55
Publication Year: 1992
CODEN: EDLEDZ ISSN: 0193-8576
Language: English
Abstract: The authors demonstrate an **antifuse** structure with a cell area of 0.2 multiplied by 0.2 mu m**2 which is fabricated by using the vertical sidewall of a polysilicon interconnect layer and two-mask patterning and etching steps. The **antifuse** is constructed in such a way that its vertical dimension is determined by the thickness of the polysilicon layer, and its horizontal dimension is determined by two-mask patterning and etching steps. For a conventional contact-**hole** type of structure, a 0.2- mu m lithographic capability will be required to achieve the same **antifuse** cell size. It is also demonstrated that the time-dependent dielectric breakdown (TDDB) reliability of this sidewall **antifuse** is as good as that of a conventional planar contact-**hole antifuse**. 3 Refs.

33/3,AB/28 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05497422 Genuine Article#: WC476 Number of References: 8
Title: 2-DIMENSIONAL MODELING FOR THE CURRENT-DENSITY DISTRIBUTION IN A HEAVILY-DOPED SEMICONDUCTOR RESISTOR (Abstract Available)
Author(s): KIM JD; KOO JG; NAM KS
Corporate Source: ELECT & TELECOMMUN RES INST,SEMICOND DIV,POB 106/TAEJON 305600//SOUTH KOREA/
Journal: INTERNATIONAL JOURNAL OF ELECTRONICS, 1997, V82, N1 (JAN), P19-25
ISSN: 0020-7217
Language: ENGLISH Document Type: ARTICLE
Abstract: A two-dimensional model for the calculation of the current density distribution in a heavily doped semiconductor resistor is described as a function of time and position along the width and length. During the initial stages of the discharge, when the total current is increasing rapidly with time, the current first appears at the **edges** of the resistor. After the initial stages, the current diffuses from the **edges** toward the centre of the device. The new model described in this paper may aid in explaining the behaviours of uneven melting and programming of semiconductor bridges and **antifuse** devices, respectively.

33/3,AB/29 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05032516 Genuine Article#: TK562 Number of References: 7

Title: INTERFACIAL REACTION IN THE SPUTTER-DEPOSITED SIO2/TI0.1W0.9 **ANTIFUSE** SYSTEM (Abstract Available)
Author(s): BAEK JT; PARK HH; CHO KI; YOO HJ; KANG SW; AHN BT
Corporate Source: ELECTR & TELECOMMUN RES INST,DIV SEMICOND TECHNOL,YUSONG PO BOX 106/TAEJON 305600//SOUTH KOREA/
Journal: JOURNAL OF APPLIED PHYSICS, 1995, V78, N12 (DEC 15), P7074-7079
ISSN: 0021-8979
Language: ENGLISH Document Type: ARTICLE
Abstract: The effects of annealing temperature on the interfacial reactions and the **antifuse** I-V characteristics of ultra thin SiO2 layer deposited on Ti0.1W0.9 substrate were investigated. The interfacial reactions were analyzed using x-ray photoelectron spectroscopy and Auger electron spectroscopy with the sample which is in situ annealed under ultra high vacuum or ex situ annealed in a nitrogen atmosphere. The surface of the Ti0.1W0.9 substrate was oxidized during sputter deposition of SiO2 layer. Ti, **W** oxides consist of Ti2O3 (Ti3O5), TiO2, WO2, and WO3. The WO3 and Ti2O3 decomposed into metallic **W** and Ti at 400 and 500 degrees C, respectively. The breakdown voltage of the **antifuse** decreased as the annealing temperature increased, due to the thinning of **dielectric layer** resulted from the decomposition of Ti, **W** oxides and the formation of metallic **W** and Ti. Annealing at 600 degrees C caused the reaction between metallic (Ti,**W**) and SiO2 layer and formed elemental silicon in the **dielectric layer**, where SiO2 **layer** completely lost its **dielectric** property. The breakdown of dielectric property might form a metallic **channel** in the SiO2 film, which mainly contains metallic **W**, Ti, and Si. (C) 1995 American Institute of Physics.

33/3,AB/30 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

04736478 Genuine Article#: UD941 Number of References: 7
Title: EXTREMELY LOW ON-RESISTANCE METAL-TO-METAL **ANTIFUSES** WITH **AL-CU**/10-NM THICK P-SINX/**AL-CU** STRUCTURE FOR NEXT-GENERATION VERY-HIGH-SPEED FPGAS (FIELD-PROGRAMMABLE GATE ARRAYS) (Abstract Available)
Author(s): TAMURA Y; KIMURA Y; TSUTSUI C; SHINRIKI H
Corporate Source: KAWASAKI STEEL CHEM IND CO LTD,ADV TECHNOL RES SECT,LARGE SCALE INTEGRAT DIV,CHUOH KU/CHIBA 260//JAPAN/
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1996, V35, N2B (FEB), P1049-1053
ISSN: 0021-4922
Language: ENGLISH Document Type: ARTICLE
Abstract: We present a novel, metal-to-metal **antifuse** structure consisting of a plasma enhanced CVD (chemical vapor deposition) **silicon nitride** (p-SiNx) **dielectric film** sandwiched between two **aluminum** layers. The leakage current in the off-state is markedly reduced by using **aluminum** film as the upper electrode instead of Ti (titanium) or TiN (titanium nitride) film. A **Al-Cu**/10 nm-thick p-SiNx/**Al-Cu** structure **antifuse** provides sufficient long-term off-state reliability exceeding ten years at 3.6 V while keeping low breakdown voltage (10 V). An extremely low on-resistance of around 3 Omega and a narrow distribution are also realized. A new **antifuse** structure (**Al-Cu**/p-SiNx/**Al-Cu**(100 nm)/Ti/TiN/**Al-Cu**) highly compatible with the conventional **via** formation

process in double metal interconnect wiring is proposed. This type of **antifuse** structure is very promising for next-generation very high-speed FPGAs.

33/3,AB/31 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01562770 AAD9718496
DEPOSITION, CHARACTERIZATION, AND DEVICE APPLICATION OF **AMORPHOUS CARBON** AND **AMORPHOUS SILICON** FILMS (**ANTIFUSES**)
Author: LIU, SHIXI
Degree: PH.D.
Year: 1987
Corporate Source/Institution: TEXAS TECH UNIVERSITY (0230)
Source: VOLUME 58/01-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 250. 221 PAGES

The purpose of this work is to develop an expertise of deposition of **amorphous carbon** (a-**C**) films, especially **diamond** -like **carbon** (DLC) films using various deposition systems, and to acquire better understandings of this material by various characterization techniques, and finally to study the feasibility of using this **material** as a new **dielectric** for Metal-to-Metal **antifuse** devices lo solve the switching problem of the **amorphous silicon** (a-**Si**) **antifuses**.

In this work, we report successful deposition of DLC films using a microwave electron cyclotron resonance (ECR) plasma system. We found that a-C:H films deposited without rf biasing are soft and polymer-like and have higher band gaps. DLC films can only be produced under a negative self-bias induced by the rf biasing. The band gap of the film decreases with the increase in rf power, and with the decrease in deposition pressure. This shows that the properties of the films depend mainly on the ion bombardment energy.

For a more in-depth investigation of **amorphous carbon**, a-C:H and its alloys (a-C:H,N,F) deposited using an rf plasma enhanced chemical vapor deposition (PECVD) system at the University of Arkansas were used. We have used infrared (IR), optical absorption, and continuous (cw) and time resolved photoluminescence (PL) to characterize these materials. We have calculated the normal mode vibrational frequencies of nitrogen and fluorine related modes using simple valence force field method. We also studied the effects of nitrogen and fluorine on the film's properties. Our optical absorption and PL data support the cluster model proposed by Robertson that a-C:H contains both sp$\sp2$ and sp$\sp3$ sites, with sp$\sp2$ clusters embedded in sp$\sp3$ bonded matrix.

For this work, a-C:H and its alloys (a-C:H,N,F) were employed as potential dielectrics for the Metal-to-Metal **antifuse** development. We found that these new **antifuses** have several characteristics superior to a-Si **antifuses** including lower values of OFF-state leakage current, ON-state resistance, dielectric constant and breakdown voltage. Most importantly, these new **antifuses** do not show ON-OFF switching which is observed in a-Si **antifuses**. Finally a phase transition model is proposed to explain the breakdown mechanism and ON-state reliability in **amorphous carbon antifuses**.

33/3,AB/32 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03647050 JICST ACCESSION NUMBER: 98A0682562 FILE SEGMENT: JICST-E
The Synergistic Inhibition Effects of Hard Base and Oxidizing Inhibitors on Pit Initiation and Growth of a Passive Film on Iron.
ARAMAKI KUNITSUGU (1); FUJIOKA EIJI (1)
(1) Keio Univ., Fac. of Sci. and Technol.
Zairyo to Kankyo(Corrosion Engineering), 1998, VOL.47,NO.7, PAGE.460-467, FIG.9, TBL.2, REF.18
JOURNAL NUMBER: F0006ABY ISSN NO: 0917-0480
UNIVERSAL DECIMAL CLASSIFICATION: 669:620.197
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The synergistic inhibition effects of a hard base, octylthiopropionate ion C8H17S(CH2)2-COO- (**OTP**-) and various oxidizing inhibitors on pit nucleation and growth were investigated for a passivated iron electrode in an aerated borate buffer solution (pH8.49) containing an aggressive anion Cl- by polarization measurements. Because the pitting potential Epit and the repassivation potential Erep were mostly shifted in the positive direction by mixtures of **OTP**- plus MoO42-, WO42-, NO3-, and NO2-, these inhibitor mixtures suppressed both pit nucleation and growth. Mixtures of **OTP**- plus CrO42- and VO3- inhibited pit initiation but stimulated pit propagation, resulting in the formation of large pits. The hard bases, **OTP**- and oxidizing inibitors suppressed pit nucleation by repairing defects in the passive film with deposits of their salts or complexes. After pit initiation, since oxidizing inhibitors like WO42- and NO3- oxidized the iron substrate surface at the bottom of a pit to change a soft acid to a hard one, they inhibited pit growth by precipitation of oxides within the pit. Inhibition of pit nucleation and growth on the passive iron surface was closely related to the hard and soft acids and bases(HSAB) principle. (author abst.)

33/3,AB/33 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03189800 JICST ACCESSION NUMBER: 97A0332765 FILE SEGMENT: JICST-E
Hardening of anodic oxidation coating of aluminium in barium hydroxide alkaline bath with addition of ion of oxygen acid.
OKUMURA KATSUTARO (1); FUJINO TAKAYOSHI (1); NOGUCHI HAYAO (1)
(1) Kinki Univ., Fac. of Sci.and Technol.
Aruminiumu Kenkyu Kaishi(Journal of the Japanese Anodizing Association), 1997, NO.2, PAGE.83-84, FIG.1, TBL.1, REF.3
JOURNAL NUMBER: F0591ABP ISSN NO: 0285-5224
UNIVERSAL DECIMAL CLASSIFICATION: 621.794
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: The anodizing was carried out in the mixed bath of Ba(OH)2 and oxoate such as sodium aluminate (SA), sodium tetraborate (S4B), and titanium potassium oxalate (**OTP**) to investigate their effect on the hardness of anodized film. The anodized film made from the bath of SA and **OTP** was not hard, while those from the bath of S4B and Ba(OH)2 were hard. Pores of diameter of 500A were observed in the

above-said four kinds of film. The hard film was made of dense cell structure.

33/3,AB/34 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

13040518 PASCAL No.: 97-0327083
A new low-resistance **antifuse** with planar metal/dielectric/poly-Si/dielectric/metal structure
Solid state devices and materials
BAEK J T; CHUNG S H; KANG S W; AHN B T; YOO H J
ARAKAWA Yasuhiko, ed; ARIMOTO Yoshihiro, ed; HATTORI Takeo, ed; HIRAYAMA Yoshiro, ed; ISHIBASHI Akira, ed; KASAHARA Kenichi, ed; KONAGAI Makoto, ed; KOYANAGI Mitsumasa, ed; MATSUMOTO Kazuhiko, ed; MIYAZAKI Seiichi, ed; NATORI Kenji, ed; ONABE Kentaro, ed; SHIBATA Tadashi, ed; SUEMUNE Ikuo, ed; TABE Michiharu, ed; TSUBOUCHI Kazuo, ed; YOKOYAMA Naoki, ed; YOSHIMI Makoto, ed
Semiconductor Technology Division, Electronics and Telecommunications Research Institute, Yusong P.O. Box 106, Taejon 305-600, Korea, Republic of ; Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology, 373-1, Koosong-dong, Yusong-gu, Taejon 305-701, Korea, Republic of
Japan Society of Applied Physics, Tokyo, Japan.
1996 International Conference on Solid State Devices and Materials (SSDM'96) (Yokohama JPN) 1996-08-26
Journal: Japanese journal of applied physics, 1997, 36 (3B p.1) 1642-1645
Language: English
A new **antifuse** with metal/dielectric/poly-Si/dielectric/metal structure has been developed for use in FPGAs as a voltage programmable link. This structure has two thermally grown dielectrics with an 8.5nm thickness and a boron-doped poly-Si pad. Low programmed on-state resistance of similar 20 OMEGA was achieved by the formation of **Al**-Si metal alloy link in the doped poly-Si pad. The metal link was formed by the diffusion of **Al** from the positive electrode into poly-Si. The dielectric property of this **antifuse** might be reliable because of no hillocks on the bottom electrode and no interaction between the thermally grown **SiO** SUB 2 and the bottom electrode.

33/3,AB/35 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

12555534 PASCAL No.: 96-0236139
Extremely low ON-resistance metal-to-metal **antifuses** with **Al**-**Cu**/10 nm-thick p-**SiN** SUB x /**Al**-**Cu** structure for next generation very high speed FPGAs : Field programmable gate arrays)
Solid state devices and materials
TAMURA Y; KIMURA Y; TSUTSUI C; SHINRIKI H
ARAKAWA Yasuhiko, ed; FUKUI Takashi, ed; FUKUMA Masao, ed; FURUYA Kazuhito, ed; ISHIWARA Hiroshi, ed; MATSUMOTO Kazuhiko, ed; MATSUMURA Masakiyo, ed; TABE Michiharu, ed; TANIGUCHI Kenji, ed; TARUCHA Seigo, ed; TSUBOUCHI Kazuo, ed; YOKOYAMA Naoki, ed
Advanced Technology Research Section, LSI division, Kawasaki Steel Corp.,

Kawasaki-cho, Chuoh-ku, Chiba 260, Japan
Institute of Industrial Science, University of Tokyo, 7-22-1 Roppongi, Minato-ku, Tokyo 106, Japan
Japan Society of Applied Physics, Tokyo, Japan.
SSDM'95. International Conference (Osaka JPN) 1995-08-21
Journal: Japanese journal of applied physics, 1996, 35 (2B p.1) 1049-1053
Language: English

We present a novel metal-to-metal **antifuse** structure consisting of a plasma enhanced CVD (chemical vapor deposition) **silicon nitride** (p-**SiN** SUB x) **dielectric film** sandwiched between two **aluminum** layers. The leakage current in the off-state is markedly reduced by using **aluminum** film as the upper electrode instead of Ti (titanium) or TiN (titanium nitride) film. A **Al-Cu**/10 nm-thick p-**SiN** SUB x /**Al-Cu** structure **antifuse** provides sufficient long-term off-state reliability exceeding ten years at 3.6 V while keeping low breakdown voltage (10 V). An extremely low on-resistance of around 3 OMEGA and a narrow distribution are also realized. A new **antifuse** structure (**Al-Cu**/p-**SiN** SUB x /**Al-Cu**(100 nm)/Ti/TiN/**Al-Cu**) highly compatible with the conventional **via** formation process in double metal interconnect wiring is proposed. This type of **antifuse** structure is very promising for next-generation very high-speed FPGAs.

33/3,AB/36 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

12341571 PASCAL No.: 95-0582776
Interfacial reaction in the sputter-deposited **SiO** SUB 2 /Ti SUB 0 SUB . SUB 1 **W** SUB 0 SUB . SUB 9 **antifuse** system
BAEK Jong Tae; PARK Hyung-Ho; CHO Kyung-Ik; YOO Hyung Joun; KANG Sang Won ; AHN Byung Tae
Semiconductor Technology Division, Electronics and Telecommunications Research Institute, Yusong P.O. Box 106, Taejon 305-600, Korea
Journal: Journal of Applied Physics, 1995-12-15, 78 (12) 7074-7079
Language: English

The effects of annealing temperature on the interfacial reactions and the **antifuse** I-V characteristics of ultra thin **SiO** SUB 2 layer deposited on Ti SUB 0 SUB . SUB 1 **W** SUB 0 SUB . SUB 9 substrate were investigated. The interfacial reactions were analyzed using x-ray photoelectron spectroscopy and Auger electron spectroscopy with the sample which is in situ annealed under ultra high vacuum or ex situ annealed in a nitrogen atmosphere. The surface of the Ti SUB 0 SUB . SUB 1 **W** SUB 0 SUB . SUB 9 substrate was oxidized during sputter deposition of **SiO** SUB 2 layer. Ti, **W** oxides consist of Ti SUB 2 O SUB 3 (Ti SUB 3 O SUB 5), TiO SUB 2 , WO SUB 2 , and WO SUB 3 . The WO SUB 3 and Ti SUB 2 O SUB 3 decomposed into metallic **W** and Ti at 400 and 500 Degree C, respectively. The breakdown voltage of the **antifuse** decreased as the annealing temperature increased, due to the thinning of **dielectric layer** resulted from the decomposition of Ti, **W** oxides and the formation of metallic **W** and Ti. Annealing at 600 Degree C caused the reaction between metallic (Ti,**W**) and **SiO** SUB 2 layer and formed elemental silicon in the **dielectric layer**, where **SiO** SUB 2 **layer** completely lost its **dielectric** property. The breakdown of dielectric property might form a metallic **channel** in the **SiO** SUB 2 film, which mainly contains metallic **W**, Ti, and Si. (c) 1995 American Institute of Physics.

33/3,AB/37 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal

12076438 PASCAL No.: 95-0278333
Novel **amorphous-silicon**-based double-metal **antifuse** with barrier enhancement layer
YEAU-KUEN FANG; KUEN-HSIEN LEE; FU-YUAN CHEN; JUN-DAR HWANG
National Cheng Kung univ., dep. electrical eng., VLSI technology lab., Tainan, Taiwan
Journal: Japanese journal of applied physics, 1995, 34 (4A p.1) 1736-1740
Language: English
The electrical characteristics, operating mechanism and reliability of a novel **amorphous-silicon**-based double-metal **antifuse** are reported in detail. A very thin alpha -SiC:H layer was inserted on both top and bottom **Al**/ alpha -Si:H interfaces as barrier enhancement layer. With proper adjustment of the thickness of this layer, the programming voltage and leakage current can be controlled. The **antifuse** offers very low on-resistance (<2 OMEGA) and low preparation temperature (<250 SUP o C), and the characteristics are independent of area, therefore, the device is suitable for integration with field-programmable gate array applications

33/3,AB/38 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

01311860 INSIDE CONFERENCE ITEM ID: CN012896050
Extremely Low ON-Resistance Metal to Metal **Antifuses** with **Al**/p-**SiN**/**Al** Structure for Next Generation FPGAs
Kimura, Y.; Tamura, Y.; Tsutsui, C.; Shinriki, H.
CONFERENCE: Solid state devices and materials-International conference
SOLID STATE DEVICES AND MATERIALS, 1995 P: 377-379
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Also known as SSDM'95. Includes papers presented at the symposium on amorphous and crystalline **insulating** thin **films** III